Layout design

- Layouts are very detailed and designing them can be very tedious and difficult.
- Layout abstractions and methodologies to help us design layouts.

Layout Design

Inverter & Its layout

Layout is drawn considering,
- Vias are used to go from n-diff to metal and then to p-diff.
- The in signal is naturally in polysilicon, but the out signal is naturally in metal, since we must use a metal strap to connect the transistors’ source and drain.
- Metal is used for the power and ground connections.
Stick diagram: Abstraction of layout

- A stick diagram is a cartoon of a layout.
- Does show all components/vias (except possibly tub ties), relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick layers

<table>
<thead>
<tr>
<th>metal 3</th>
<th>metal 2</th>
<th>metal 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>poly</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ndiff</td>
<td></td>
<td></td>
</tr>
<tr>
<td>pdiff</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dynamic latch stick diagram

Hirarchical: Sticks design of multiplexer

- Start with NAND gate:
NAND sticks

One-bit mux sticks

3-bit mux sticks

Layout design and analysis tools

- Layout editors are interactive tools.
- Design rule checkers are generally batch---identify DRC errors on the layout.
- Circuit extractors extract the netlist from the layout.
- Connectivity verification systems (CVS) compare extracted and original netlists.
Automatic layout

- Cell generators (macrocell generators) create optimized layouts for ALUs, etc.
- Standard cell/sea-of-gates layout creates layout from predesigned cells + custom routing.
  - Sea-of-gates allows routing over the cell.

Standard cell layout

[Diagram of standard cell layout with routing areas]