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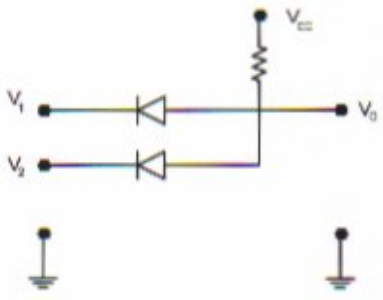
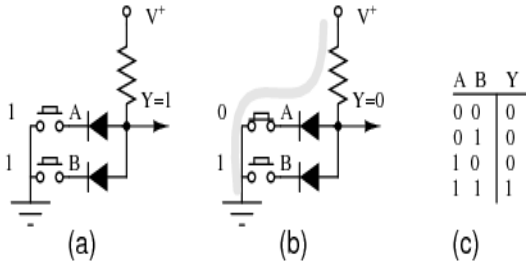
# Logic Families

- RTL – Resistor-Transistor Logic
- DTL – Diode-Transistor Logic
- TTL – Transistor-Transistor Logic
- ECL – Emitter-Coupled Logic
- MOS – Metal-oxide semiconductor
- CMOS – Complementary MOS

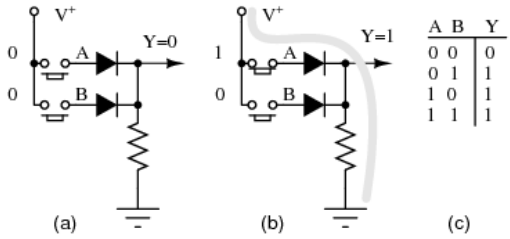
## Diode based Logic




## Diode based Logic



## Diode based Logic

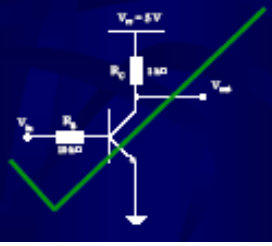



## Bipolar Digital Gate Circuits

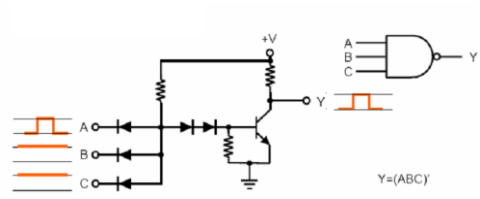
- The first forms of the digital ICs to receive general usage were BJT inverter circuits in earlier 1960s.
  - Circuits consisted of only resistors and transistors,
  - named *resistor-transistor logic (RTL)*.
- IC development a short time later consisted of a diode AND circuit followed a bipolar transistor inverter.
  - termed *diode-transistor logic (DTL)*

## Transistor Based Logic

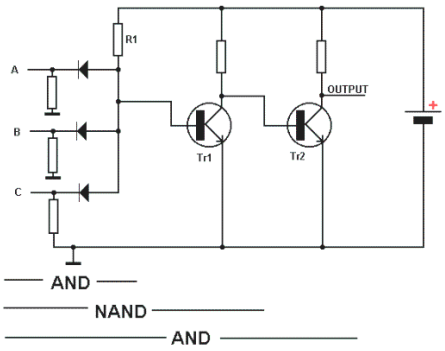
- Can use bipolar transistors



## DTL



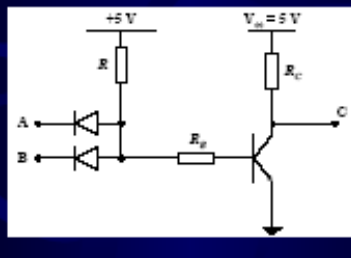
## DTL




## Resistor Transistor Logic

A diode AND network can be merged with an inverter

- Forms a diode-transistor NAND gate

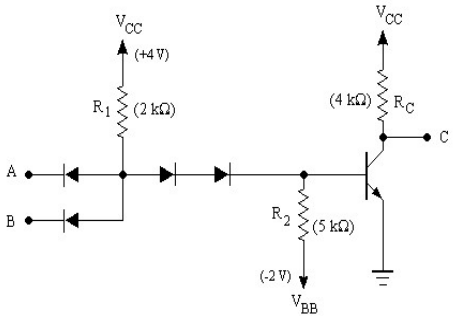


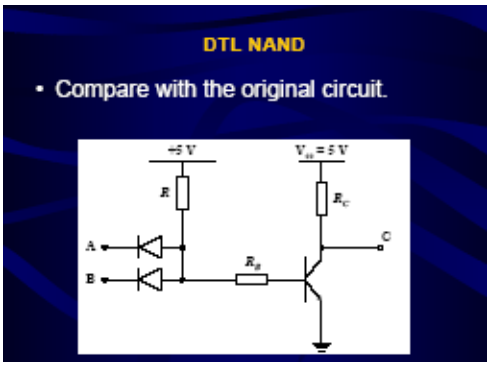

## Bipolar Digital Gate Circuits

- Choice of logic family for design of a specific digital system influenced by many factors.
  - Need for low power
  - High speed
  - Availability of more complex functions (MSI)
  - Compatibility with other parts of the system
  - cost
- Many system designs mix logic families
  - e.g. TTL and CMOS

- In the mid – late 1960's use of resistors, diodes and transistors began to disappear
  - Discrete components phased out due to new fabrication processes
  - Processes where entire circuits could be made onto one chip
- The first to appear were small scale integration SSI
  - 1 to 10 gates or memory elements packaged as a unit
  - packaged as DIL package
- MSI medium scale integration
  - 10 to 100 gates or memory elements packaged as a unit
- LSI large scale integration
  - 100 to 10000 gates or memory elements packaged as a unit
- For MSI and LSI the popular logic family is TTL

## DTL NAND



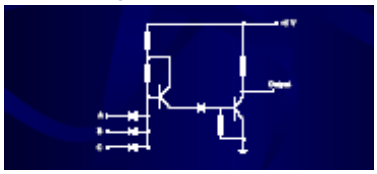

## DTL

**The extra transistor adds amplification to increase fan-out**

**– kept in the active region when output transistor is saturated**

**• Modified circuit can supply large amount of base current to the output transistor.**

**– Thus output transistor can now draw a large**

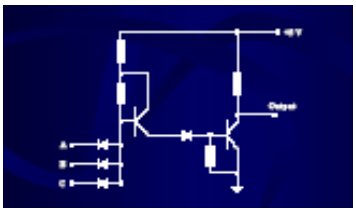


## DTL

**Part of the collector current comes from the conducting diodes in the loading gates (when the output transistor is saturated).**

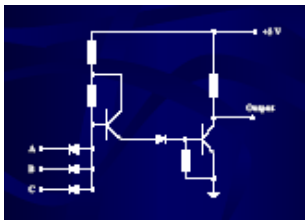
**⇒ an increase in allowable collector saturated current allows more loads to be connected to the output.**

**⇒ increase fan-out capability.**



## DTL

- Extra diode is used to provide biasing for output transistor
  - Avoids use of resistors
  - and also the need for separate negative power supply



## DTL -> TTL

- The first change from DTL to TTL:
  - In IC's it is easier to fabricate transistors than diodes.
  - When diodes are required transistors are used

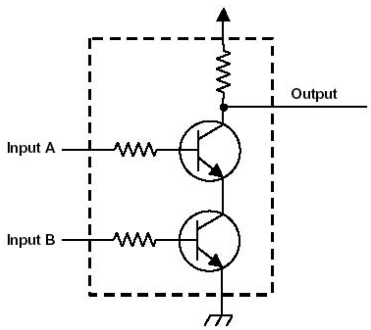
⇒ Usual to use the base-emitter junction of BJT

∴ base serving as the anode

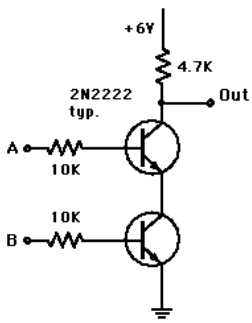
∴ emitter serving as the cathode

∴ collector tied to the base

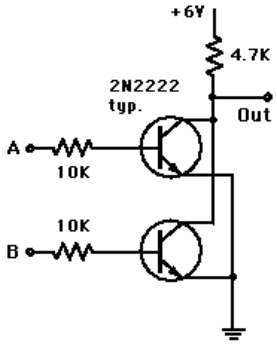
## TTL: NAND



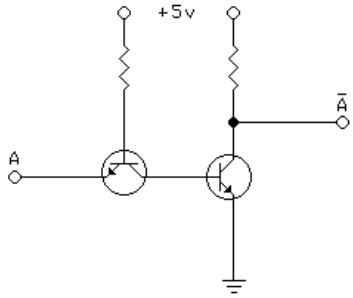

## TTL: NAND



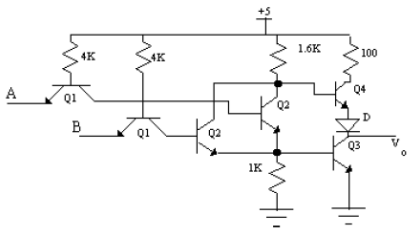
## TTL: NOR



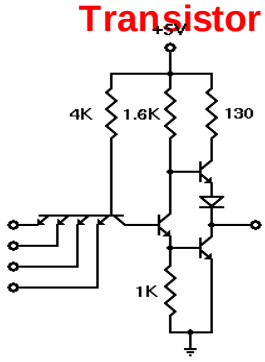

## TTL: NOR/NOT



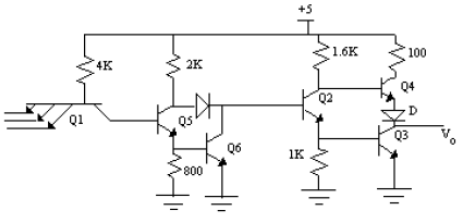

## TTL NOR gate implementation




## TTL: Multi-Emitter Transistor

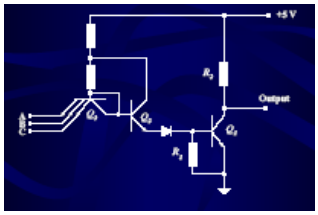


## TTL AND gate implementation



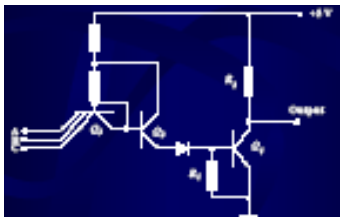

## TTL: Multi-Emitter Transistor

- Note anodes of the input diodes are common
  - Thus can be realised in the form of a multiple-emitter transistor



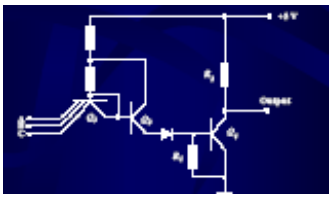
## TTL : Increase Switching Speed

- The remaining changes in the evolution from DTL to TTL made to achieve increased speed.
- When circuit is to switch from a low-output to a highoutput state.
  - Q1 must go from saturation to cut-off
  - Requires removal of charge from base of Q1



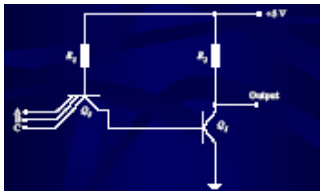
## TTL : Increase Switching Speed

- Therefore this switching action is brought about by Q2
  - Q2 going from saturation to cut-off
- The only path for discharging the base of Q1 through resistor R1.
- Speed of discharge is limited by time constant of circuit



## TTL : Faster Switching

To obtain faster switching
- Take advantage of input diodes being realised in terms of transistors
- change the circuit the following




## How to increase speed ?

Whatever is done to the value of the resistors

• Speed is ultimately limited by the time required to pull the output transistors out of saturation.

• 74, 74L and 74H series all operate with saturated switching
- many of the transistors, when conducting will be in a saturated condition

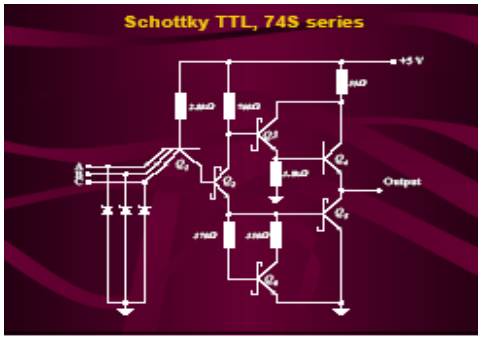
• As has been seen this causes a saturation delay (storage delay), when switching from ON to OFF
- limits the circuit's switching speed.

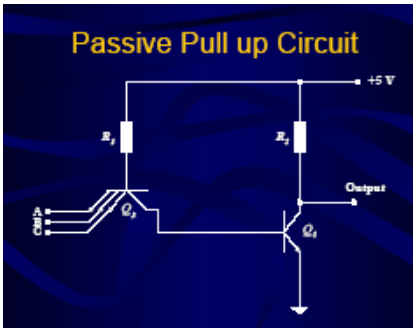
## Schottky TTL, 74S series

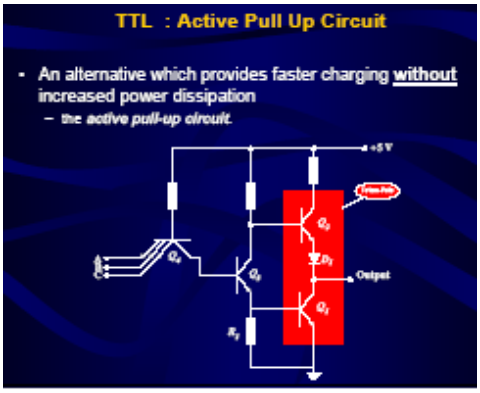
In Schottky TTL (STTL) • Transistors kept out of saturation by using Schottky barrier diodes (SD)
• Formed by a junction of a metal and semiconductor
- conventional diode with a junction of *p*-type and *n*-type semiconductor material
- SD connected between the base and the collector
- Do not allow the transistors to go as deeply into saturation
- SD has a forward voltage drop of 0.4V

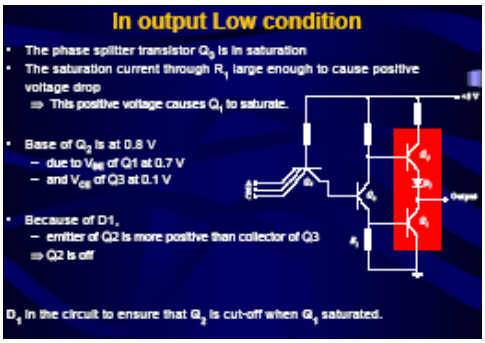
### Schottky TTL, 74S series

- When the Collector-Base junction becomes forward biased at the on-set of saturation
  - ⇒ SD will conduct, diverting some input current away from base.
  - ⇒ this has effect of reducing the excess base current.
  - ⇒ decreases saturation (storage time) delay at turn-off
- 74S00 NAND has average propagation delay of 3 nsecs
  - twice as fast as the 74H00
  - makes the 74H series redundant nowadays


Schottky TTL, 74S series
+5 V
Output

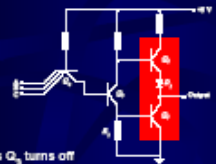

Passive Pull up Circuit
+5 V
Output


TTL : Active Pull Up Circuit
An alternative which provides faster charging without increased power dissipation
the active pull-up circuit.
+5 V
Output


In output Low condition
The phase splitter transistor Q3 is in saturation
The saturation current through R1 large enough to cause positive voltage drop
⇒ This positive voltage causes Q1 to saturate.
Base of Q2 is at 0.8 V
due to VBE of Q1 at 0.7 V
and VCE of Q3 at 0.1 V
Because of D1,
emitter of Q2 is more positive than collector of Q3
⇒ Q2 is off
D1 in the circuit to ensure that Q4 is cut-off when Q3 saturated.

## In output High condition

- Output High due to one of the inputs dropping low
  ⇒ Q3 and Q1 go into cut-off
- However output remains momentarily low
  – as voltage across load capacitance cannot change instantaneously



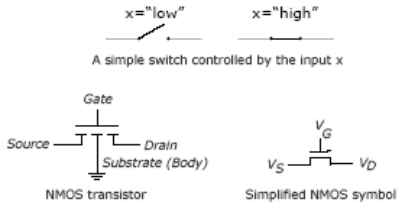
- As soon as $Q_5$ turns off
  ⇒ $Q_5$ conducts as its base is connected to $V_{CC}$ via resistor.
- Current needed to charge load capacitance causes $Q_2$ to momentarily saturate
  ⇒ output voltage rises with a time constant RC

## Transistor switches

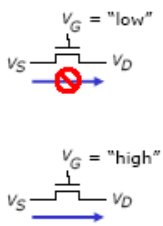
- Logic circuits are built with transistors
- We will assume a transistor operates as a simple switch controlled by a logic signal x
- The most popular type of transistor for implementing a simple switch is the ***metal oxide semiconductor field effect transistor*** (MOSFET)
- Two types of MOSFETs
  - N-channel (***NMOS***)
  - P-channel (***PMOS***)
- Early circuits relied on NMOS or PMOS transistors, but not both
- Current circuits use both NMOS and PMOS transistors in a configuration called ***complementary MOS*** (CMOS)



## NMOS transistor as a switch

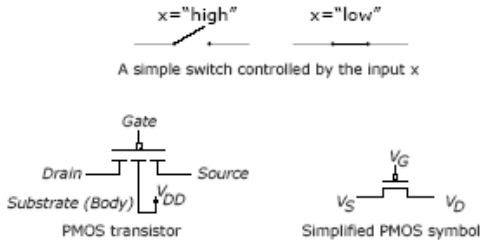



## NMOS transistor as a switch

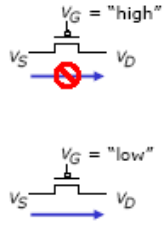



- The transistor operates by controlling the voltage $V_g$ at the gate terminal
- If $V_g$ is low, there is no connection between the source and the drain terminals. The transistor is ***turned off***.
- If $V_g$ is high, the transistor is ***turned on*** and acts as a closed switch between the source and drain terminals.

## PMOS transistor as a switch




## PMOS transistor as a switch

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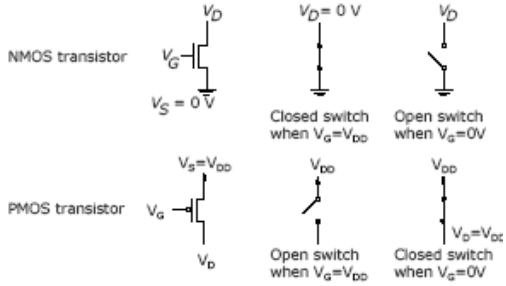
## NMOS and PMOS in logic circuits



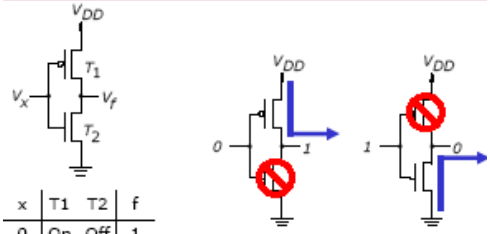

## NMOS and PMOS in logic circuits

- When the NMOS transistor is turned on, its drain is ***pulled down to Gnd***
- When the PMOS transistor is turned on, its drain is ***pulled up to $V_{DD}$***
- Because of the way transistors operate:
  - An NMOS transistor cannot be used to pull its drain terminal completely up to $V_{DD}$
  - A PMOS transistor cannot be used to pull its drain terminal completely down to Gnd
- Therefore, NMOS and PMOS transistors are commonly used in pairs in CMOS circuits

## CMOS logic gates

- A CMOS logic gate involves NMOS transistors in a ***pull-down network*** (PDN) and PMOS transistors in a ***pull-up network*** (PUN)
- The functions realized by the PDN and PUN networks are complements of one another
- The PDN and PUN have equal numbers of transistors, which are arranged so that the two networks are duals of one another
  - Wherever the PDN has NMOS transistors in series, the PUN has PMOS transistors in parallel, and vice versa

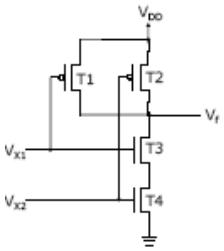
## CMOS NOT gate




| x | T1 | T2 | f |
|---|---|---|---|
| 0 | On | Off | 1 |
| 1 | Off | On | 0 |

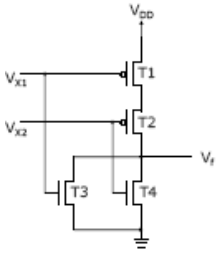
2 transistors

## CMOS NAND gate




| X1 | X2 | T1 | T2 | T3 | T4 | f |
|---|---|---|---|---|---|---|
| 0 | 0 | On | On | Off | Off | 1 |
| 0 | 1 | On | Off | Off | On | 1 |
| 1 | 0 | Off | On | On | Off | 1 |
| 1 | 1 | Off | Off | On | On | 0 |

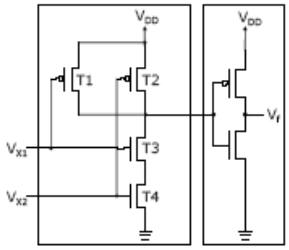
## CMOS NOR gate




| X1 | X2 | T1 | T2 | T3 | T4 | f |
|---|---|---|---|---|---|---|
| 0 | 0 | On | On | Off | Off | 1 |
| 0 | 1 | On | Off | Off | On | 0 |
| 1 | 0 | Off | On | On | Off | 0 |
| 1 | 1 | Off | Off | On | On | 0 |

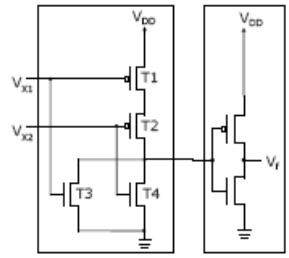
4 transistors

## CMOS AND gate




6 transistors

## CMOS OR gate




6 transistors