Dept. of Computer Science and Engineering
University of Rajshahi
www.ru.ac.bd

Dr. Shamim Ahmad

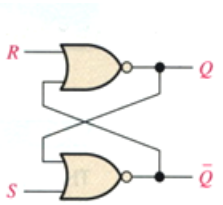
4 Basic types of Flip-Flops

- **SR, JK, D, and T**
- JK ff has
  - 2 inputs, J and K
  - Need to be asserted at the same time to change the state
- D ff has
  - 1 input D (DATA)
  - Which sets the ff when D = 1 and resets it when D = 0

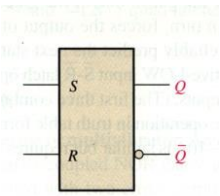
4 Basic types of Flip-Flops

- T ff has
  - 1 input T (Toggle)
  - Which forces the ff to change states when T = 1
- SR ff has
  - 2 inputs, S (set) and R (reset)
  - That set or reset the output Q when asserted

SR FF (active HIGH)

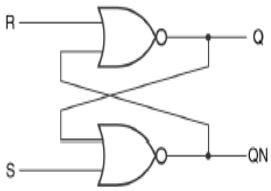


(a) Active-HIGH input S-R latch



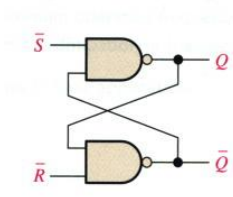
(a) Active-HIGH input S-R latch

SR FF NOR gate

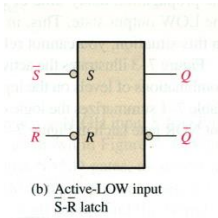


S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

SR FF (active LOW)

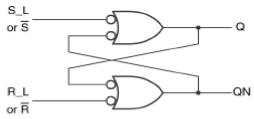


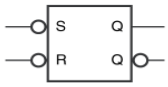
(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch



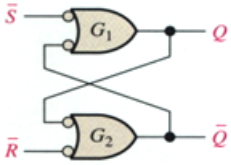
(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

SR FF (NAND gate)





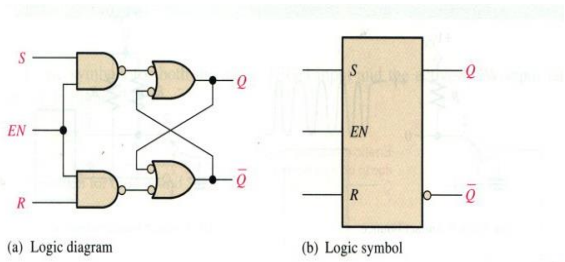
S_L	R_L	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	last Q	last QN



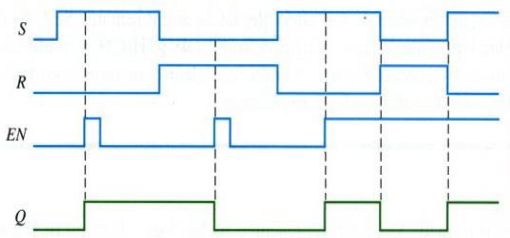
SR FF Truth Table

INPUTS $\bar{S}$	INPUTS $\bar{R}$	OUTPUTS Q	OUTPUTS $\bar{Q}$	COMMENTS
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

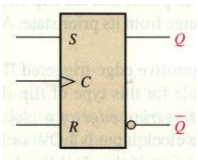
SR FF with Enable input

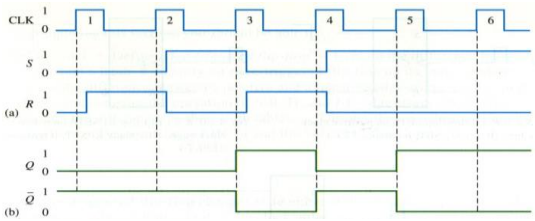


The Gated S-R Latch



Edged-Triggered S-R FF

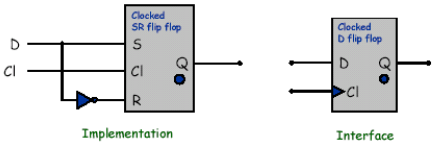


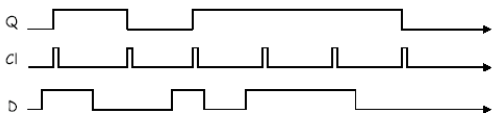


Clocked D Flip-Flop

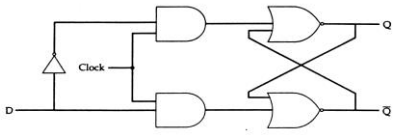
Clocked D Flip-Flop.

- Output follows D input while clock is 1.
- Output is remembered while clock is 0.



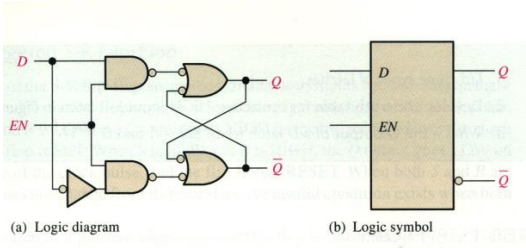


Gated D-Latch



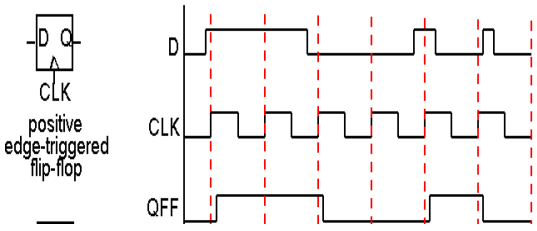
- **Ensures S and R inputs never equal to 1 at the same time**
- **Useful in control application where setting or resetting a flag to some condition is needed**
- **Stores bits of information**
- **Constructed from a gated SR latch and a Data latch**

The Gated D Latch

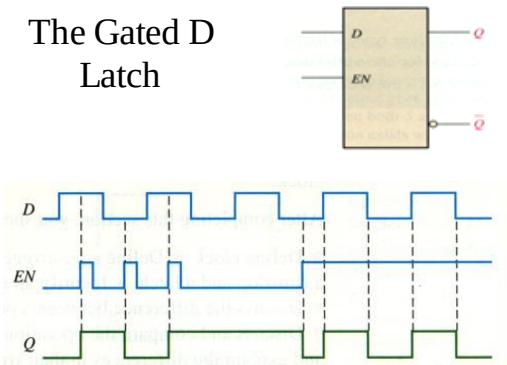


(a) Logic diagram (b) Logic symbol

Positive edge-triggered D FF

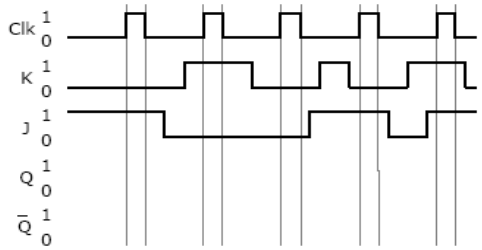


The Gated D Latch



JK flip-flop timing diagram

Complete the following timing diagram



Edge-Triggered D FF

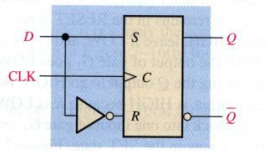
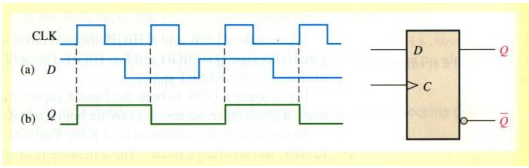


TABLE 7–3
Truth table for a positive edge-triggered D flip-flop.

INPUTS		OUTPUTS		COMMENTS
D	CLK	Q	$\overline{Q}$	
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock trinsition LOW to HIGH

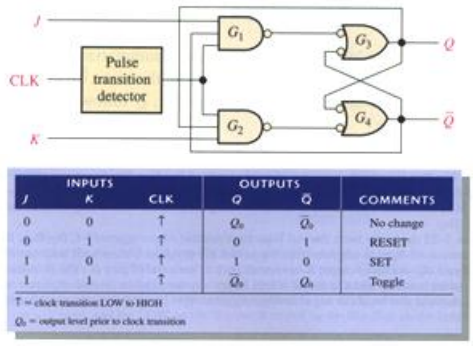
Edge-Triggered D FF



Edge-Triggered JK-FF

- JK-FF is versatile and is a widely used type of flip-flop.
- The functioning of the JK-FF is identical to that of the SR-FF in the SET, RESET, and NC.
  - The **difference** is that the JK-FF **has NO invalid state** as does the SR-FF.

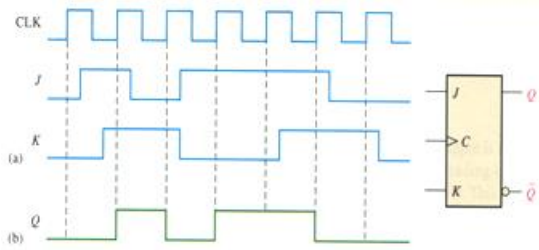
Edge-Triggered JK-FF



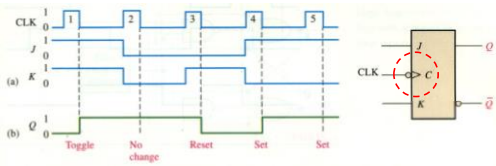
INPUTS J	K	CLK	OUTPUTS Q	$\bar{Q}$	COMMENTS
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH
Q_0 = output level prior to clock transition

Edge-Triggered JK-FF

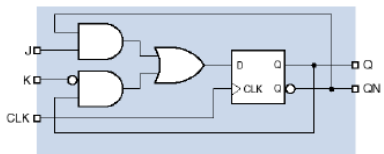


Edge-Triggered JK-FF



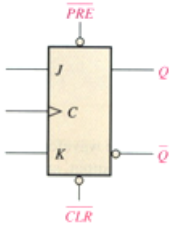
Edge-Triggered J-K flip-flop

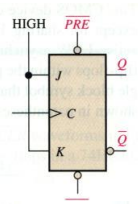
J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q



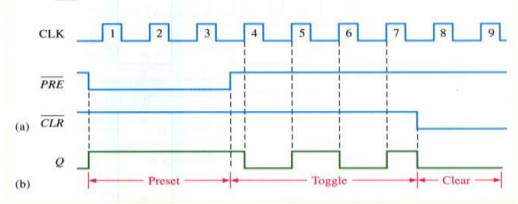
Asynchronous Preset and Clear Inputs

- Most IC flip-flops have **asynchronous** inputs.
  - These are inputs that affect the state of the FF **independent of the clock**.
  - Preset (PRE) or direct set (S_D)
  - Clear (CLR) or direct reset (R_D)



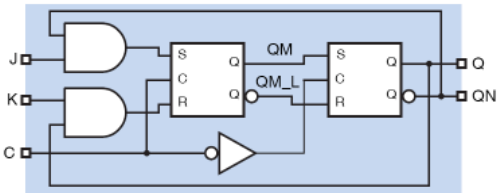


Edge-triggered JK-FF with PRE and CLR



Master/slave J-K flip-flop (Pulse triggered)

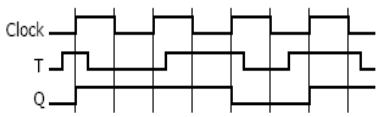
J	K	C	Q	QN
x	x	0	last Q	last QN
0	0	⎍	last Q	last QN
0	1	⎍	0	1
1	0	⎍	1	0
1	1	⎍	last QN	last Q

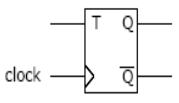


T flip-flop

- The name T derives from the behavior of the circuit, which 'toggles' its state when T=1
  - This feature makes the T flip-flop a useful element when constructing counter circuits

T	Q(t+1)
0	Q(t)
1	Q'(t)





Positive edge triggered