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Digital IC Terminology

- Current and voltage parameters
- Fan-Out
- Propagation delays
- Power requirements
- Noise immunity
- Invalid voltage levels
- Current-sourcing and current-sinking action
- IC Packages

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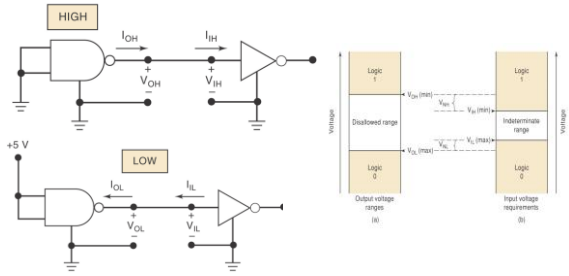
Current and voltage parameters



Currents and voltages in the two logic states

Current and voltage parameters
Voltage Levels

- **V_{IH}(min):** High Level Input Voltage : minimum voltage level required for logic 1 at an input
- **V_{IL}(max):** Low Level Input Voltage : maximum voltage level required for logic 0 at an input
- **V_{oH}(min):** High Level Output Voltage : minimum voltage level at an output for logic 1 state
- **V_{OL}(max):** Low Level Output Voltage : maximum voltage level at an output for logic 1 state

Current and voltage parameters
Current Levels

- **I_{IH}:** High Level Input Current : Current flowing into an input at a logic state 1
- **I_{IL}:** Low Level Input Current : Current flowing into an input at a logic state 0
- **I_{OH}:** High Level Output Current : Current flowing from an output at logic state 1
- **I_{OL}:** Low Level Output Current : Current flowing from an output at logic state 0

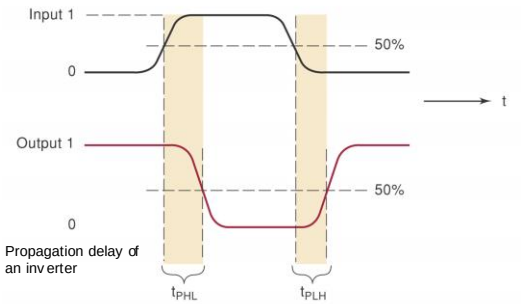
Fan-Out

- Maximum number of logic inputs that an output can drive reliably
- Depends on the logic family
- Example: a logic gate specified with a fan-out of 10, can drive 10 logic inputs. If this is exceeded, the output logic levels cannot be guaranteed

Propagation Delay

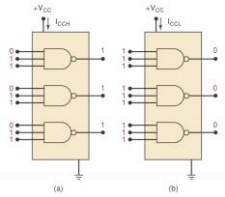
- Delay encountered by a signal in going through a circuit
  - t_{PLH} delay time in going from logic 0 to logic 1
  - t_{PHL} delay time in going from logic 1 to logic 0
- t_{PLH} and t_{PHL} are not necessarily the same values
- Propagation Delay is a measure of the relative speed of logic circuits. The smaller the delay, the faster the circuit

Propagation Delay



Power Requirements

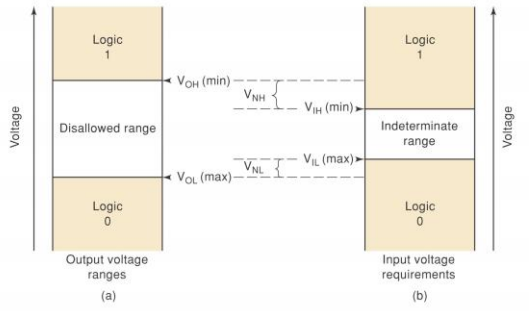
- **Power pin**
  - (V_{CC} for TTL, V_{DD} for MOS devices)
- **Power required**=
  - I_{CC}* V_{CC} or V_{DD}*I_{DD}
- **Average Current**
  $I_{CC(avg)}=(I_{CCH}+I_{CCL})/2$
- **P(avg)=** $I_{CC(avg)}$ * V_{CC}



Noise Immunity

- **High-state noise margin,**
  $V_{NH}= V_{OH}(min) – V_{IH}(min)$
  Negative noise spikes greater than V_{NH} can cause the voltage to drop into the indeterminate range
- **Low-state noise margin,**
  $V_{NL}= V_{IL}(max)- V_{OL}(max)$
  Positive noise spikes greater than V_{NL} can cause the voltage to rise into the indeterminate range

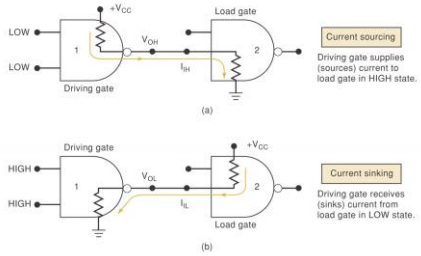
Noise Immunity



Invalid Voltage Levels

- Proper operation requires the input voltages be kept outside the indeterminate range
  - (**less than V_{IL}(max) or greater than V_{IH}(min)**
- Voltage output (connected to an input) could be outside the valid region due to malfunctioning or being overloaded (**fan-out exceeded**)
- Power supply voltages **outside acceptable range** can cause invalid voltage levels.

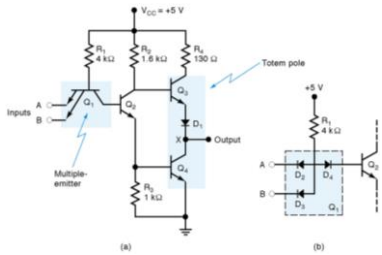
Current-Sourcing and Current- Sinking Action



An output must be able to source or sink a current when connected to an input

The TTL Logic Family

- The NAND gate is a basic TTL circuit.



The TTL Logic Family

- **Current sinking action:**
  A TTL output acts as a **current sink** in the low state
- **Current sourcing action:**
  A TTL output acts as a **current source** in the high state

The TTL Logic Family

- TTL circuits have a similar structure
- The input will be the **cathode** of a PN junction
  - A **HIGH input** will turn off the junction and only a leakage current is generated.
  - A **LOW input** turns on the junction and a relatively large current is generated
- Most TTL circuits have some type of totem-pole output configuration

TTL Data Sheets

- First line of TTL ICs was the **54/74** series
  - 54 series operates over a wider temperature range
- Same numbering system, **prefix** indicates manufacturer
  - **SN** – Texas Instruments
  - **DM** – National Semiconductor
  - **S** – Signetics
  - DM7402, SN7402, S7402 all perform the same function
- Data sheets contain electrical characteristics, switching characteristics, and recommended operating conditions.

TTL Data Sheets

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies over temperature range −55°C to 70°C
§ Applies over temperature range 70°C to 125°C

TTL Data Sheets

electrical characteristics over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TTL Data Sheets

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54ALS00A		SN74ALS00A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	15	3	11	ns
t_{PHL}			2	9	2	8	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

TTL Series Characteristics

- Standard 74 series TTL has evolved into other series:
  - **Standard** TTL, **74** series
  - S**chottky** TTL, 74**S** series
  - **Low power Schottky** TTL, 74**LS** series (LS-TTL)
  - **Advanced Schottky** TTL, 74**AS** series (AS-TTL)
  - **Advanced low power** Schottky TTL, 74ALS series
  - **74F fast** TTL

TTL Series Characteristics

TABLE 8-6 Typical TTL series characteristics.

	74	74S	74LS	74AS	74ALS	74F
Performance ratings						
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Speed–power product (pJ)	90	60	19	13.6	4.8	18
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
V_{OH}(min)	2.4	2.7	2.7	2.5	2.5	2.5
V_{OL}(max)	0.4	0.5	0.5	0.5	0.5	0.5
V_{IH}(min)	2.0	2.0	2.0	2.0	2.0	2.0
V_{IL}(max)	0.8	0.8	0.8	0.8	0.8	0.8

TTL Loading and Fan Out

- **Fan out** refers to the load drive capability of an IC output
  - A TTL output **has a limit** on how much current it can **sink in the LOW** state
  - A TTL output has a **limit on how** much current it **can source** in the HIGH state.
  - Exceeding these currents will result in output voltage levels outside specified ranges

TTL Loading and Fan Out

- Determining fan out
  - Add the I_{IH} for all inputs connected to an output. The sum must be less than the output I_{OH} specification.
  - Add the I_{IL} for all inputs connected to an output. The sum must be less than the output I_{OL} specification.
  - See example 8-5 page 510

TTL Loading and Fan Out

- Determining fan out :

How many 74ALS00 NAND gate inputs can be driven by a 74ALS00 NAND gate output?

I_{oL}(max)=8 mA **I_{IL}(max)=**0.1 mA
fan-out (low)= I_{oL}(max)/ I_{IL}(max)=8/0.1=80
I_{oH}(max)=0.4 mA=400µA **I_{IH}(max)=**20µA
fan-out (high)= I_{oH}(max)/ I_{IH}(max)=400/20=20

Choose the smaller:Fan-out=20

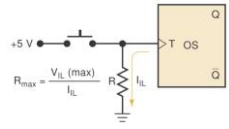
Therefore, the 74ALS00 NAND gate can drive up to 20 other 74ALS00 NAND gates

Other TTL Characteristics

- **Unconnected (floating) inputs:** an input left unconnected acts like a logic 1 applied to that input.
- Unused inputs: (will pick noise)
- Tied together inputs : Input current = sum of individual currents single current for NAND/AND gates in low states
- Current transients
  - When a totem pole TTL output goes from LOW to HIGH, a high amplitude current spike is drawn from the V_{CC} supply
  - Ceramic disk capacitors (.01 or .1 µF) are used to short these high frequency spikes to ground.

Other TTL Characteristics

- Biasing TTL inputs Low R is needed to keep the T input low while the switch is open



Voltage drop across R should be less than V_{IL} (max)
R_{max}= (V_{IL}(max)/I_{IL}
R is chosen slightly below R_{max} to reduce current drain

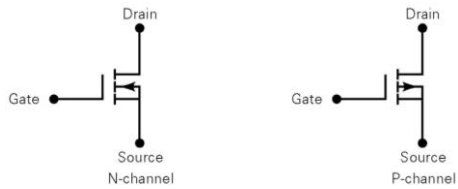
- Example: (V_{IL}(max) = 0.8 V I_{IL} =0.4 mA
R_{max} =0.8V/0.4mA = 2000 Ω
Choose R=1.8kΩ (standard resistor)

MOS Technology

- Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)
  - Simple and cheap to fabricate
  - Consume very little power
  - More circuit elements are possible
  - Susceptible to static electricity damage

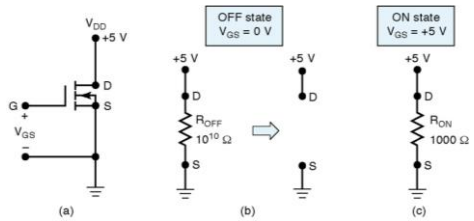
MOS Technology

- Schematic symbols for P and N channel enhancement MOSFETs.



MOS Technology

- The basic MOSFET switch



Complementary MOS Logic

- **P-MOS** – uses only P channel enhancement MOSFETs
- **N-MOS** – uses only N channel enhancement MOSFETs
- **CMOS** – uses both P and N channel devices
  - Faster
  - Consumes less power
  - More complex fabrication

Complementary MOS Logic

TABLE 8-9 Input/output voltage levels (in volts) with $V_{DD} = V_{CC} = +5$ V.

	CMOS							TTL		
Parameter	4000B	74HC	74HCT	74AC	74ACT	74AHC	74AHCT	74	74LS	74AS
V_{IH}(min)	3.5	3.5	2.0	3.5	2.0	3.85	2.0	2.0	2.0	2.0
V_{IL}(max)	1.5	1.0	0.8	1.5	0.8	1.65	0.8	0.8	0.8	0.8
V_{OH}(min)	4.95	4.9	4.9	4.9	4.9	4.4	3.15	2.4	2.7	2.7
V_{OL}(max)	0.05	0.1	0.1	0.1	0.1	0.44	0.1	0.4	0.5	0.5
V_{NH}	1.45	1.4	2.9	1.4	2.9	0.55	1.15	0.4	0.7	0.7
V_{NL}	1.45	0.9	0.7	1.4	0.7	1.21	0.7	0.4	0.3	0.3

CMOS Series Characteristics

- CMOS devices compete directly with TTL
  - Pin compatible
  - Functionally equivalent
  - Electrically compatible
- 4000/1400 series
- 74C series
- 74HC/HCT (high-speed CMOS)
  are functionally and pin compatible with TTL IC's with the same name. The HCT is also electrically compatible with TTL

CMOS Series Characteristics

- 74AC/ACT (advanced CMOS)
- 74AHC/AHCT (advanced high-speed CMOS)
- BiCMOS 5-volt logic

CMOS Series Characteristics

- **P_D** increases with frequency
- **Fan out (large)**
- **Switching speed**
- Unused inputs (will pick static, cause heat, invalid output). Unused inputs should be connectd to 0V or V_{DD} or another input
- Static sensitivity
  - ESD precautions
- Latch up

Low Voltage Technology

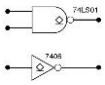
- CMOS family:
  - 74LVC (low voltage CMOS)
  - 74ALVC (advanced low voltage CMOS)
  - 74LV (low voltage)
  - 74AVC (advanced very low voltage CMOS)
  - 74AUC (advanced ultra-low voltage CMOS)
  - 74AUP (advanced ultra-low power)
  - 74CBT (cross bar technology)
  - 74CBTLV (cross bar technology low voltage)
  - 74GTLP (gunning transceiver logic plus)
  - 74SSTV (stub series terminated logic)
  - 74TVC (translation voltage clamp)

Low Voltage Technology

- BiCMOS family:
  - 74LVT (low voltage BiCMOS technology)
  - 74ALVT (advanced low voltage BiCMOS technology)
  - 74ALB (advanced low voltage BiCMOS)
  - 74VME (VERSA Module Eurocard)
- The move toward low voltage systems will continue and the technician must be prepared to operate in an environment where devices may not necessarily operate on 5 volts.

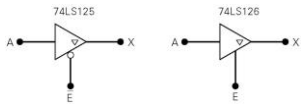
Open Collector/Open Drain Outputs

- Conventional CMOS outputs and TTL totem pole outputs should never be connected to the same point. (will fight each other)
- **Open-collector/open-drain** outputs (need an external pull-up resistor to V_{CC}. (the pull-up transistor of the totem pole is removed)
- Open-collector/open-drain buffer/drivers
- IEEE/ANSI symbols for open collector/drain outputs



Tristate (Three-State) Logic Outputs

- Three states are possible: HIGH, LOW, and high impedance.
- Advantages of tristate devices
- Tristate buffers
- Tristate ICs
- IEEE/ANSI symbol for tristate outputs



High-Speed Bus Interface Logic

- At **high frequencies** bus wires of more than about 4 inches in length act like transmission lines.
- In order to prevent **reflected waves**, the end of a bus must be terminated with a resistance equal to the line impedance (about 50 Ohms).
- Figure 8-40 illustrates termination techniques.

The ECL Digital IC Family

- Emitter coupled logic – increases switching speed.
- Basic ECL circuit
- ECL OR/NOR gate
- ECL characteristics
  - Very fast switching, typical propagation delay is 360 ps
  - -0.8 V logic 1, -1.7 V logic 0
  - Noise margins approximately 150 mV
  - Output complement is produced, eliminating need for inverters
  - **Typical fan out is 25**
  - Typical power dissipation is 25 mW
  - Current flow remains constant, eliminating noise spikes

CMOS Transmission Gate (Bilateral Switch)

- **Acts as a single pole, single throw switch**
- Controlled by an input logic level
- Passes signals in both directions
- Signals applied to the input can be analog or digital
- Input must be between 0 and V_{DD} volts.

IC Interfacing

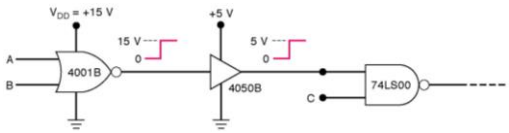
- **Driver** – provides the output signal.
- **Load** – receives the signal.
- **Interface circuit** – connected between driver and load to condition the signal for the load.
  - Interfacing between logic families is common in digital systems.
-

Interfacing 5-V TTL and CMOS

- TTL easily meets **CMOS input current** requirements. CMOS can **drive TTL loads.**
- TTL output voltage must be **raised** for input to some CMOS devices. The most common solution is a pull-up resistor.

Interfacing 5-V TTL and CMOS

- CMOS output for both logic states
- CMOS driving TTL in the HIGH state
- CMOS driving TTL in the LOW state
- High voltage CMOS driving TTL



Analog Voltage Comparators

- Useful in systems with analog and digital components
- Compares two voltages. If voltage on the (+) input is greater than (-) input the output is high. If input on the (-) is greater the output is low.
- May be considered a one bit analog to digital converter.
-

Troubleshooting

- Logic pulser – tool that generates a short pulse when actuated
  - Senses the existing voltage level and produces a pulse in the opposite polarity
  - Output impedance of 2 Ohms or less
- Using logic pulser and probe to test a circuit
- Finding shorted nodes