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PAL and PLA

- Programmable Array Logic (PAL)
- Monolithic Memories, Inc. (MMI)
- March 1978
- Registered trademark on the term PAL
- "Programmable Semiconductor Logic Circuits".
- The trademark
  - Currently held by Lattice Semiconductor

- **Signetics**
  - Field programmable logic array (FPLA)
  - 1975
  - Unfamiliar to most circuit designers
  - Perceived to be too difficult to use
  - Slow maximum operating
  - Large package, a 600-mil (0.6", or 15.24 mm) wide 28-pin

PAL devices consisted of a small PROM

- One-time programmable
- Hard array logic
  - mask-programmed at the factory
- UV erasable versions
  - PALCxxxxx, Example PALC22V10
-

PAL devices consisted of a small PROM

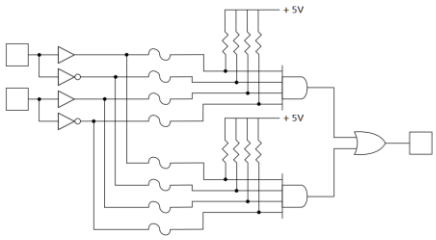
- Flash erasable devices
  - PALCExxx, Example: PALCE22V10
  - Electrically-erasable
- GAL : Generic array logic, gate array logic
  - Lattice Semiconductor
  - AMD
  - National Semiconductor
  - GAL22V10

Bipolar transistor technology

- Early PALs were 20-pin DIP components
- One-time programmable (OTP) titanium-tungsten programming
- Lattice Semiconductor

CMOS Technology.

- Cypress
- Lattice Semiconductor
- Advanced Micro Devices (AMD)



Simplified programmable logic device

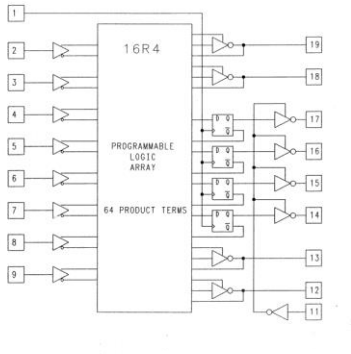
True and complemented inputs to the AND gates.

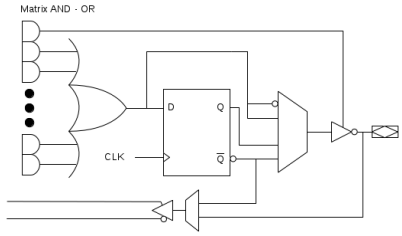
"Fixed-OR, Programmable-AND"
AND gates -> product terms,
OR gates -> sum-of-products logic array.

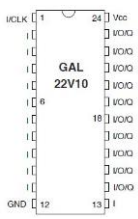
Programmable logic plane

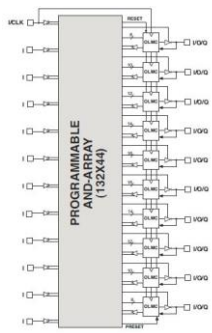
- The programmable logic plane is a programmable read-only memory
  - That allows the signals present on the device pins
  - The logical complements of those signals
  - To be routed to output logic ro macrocells

- **Output logic**
  - The early 20-pin PALs had 10 inputs and 8 outputs.
  - The outputs were active low
    - Registered
    - Combinational.







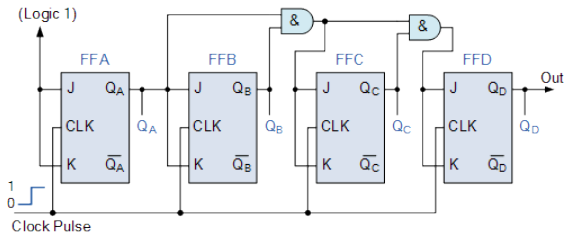


- PAL16L8
  - 8 combinational outputs
- PAL16R8
  - 8 registered outputs
- PAL16R6
  - 6 registered and 2 combinational
- PAL16R4
  - 4 registered and 4 combinational

- **22V10**
  - 24 pin device with 10 output logic macrocells
  - Each macrocell
  - Combinational
  - Registered
  - Active high
  - Active low.
  - The number of product terms allocated to an output varied from 8 to 16
- **PAL16V8, PAL20V8**

The PALASM (from "PAL assembler")

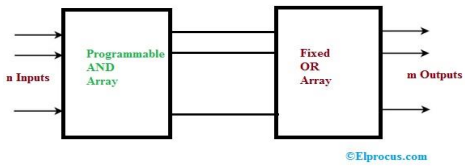
```
PAL16R4 PAL              PAL DESIGN SPECIFICATION
CNT4SC
4 bit counter with synchronous clear
Michael Holley and Dave Pellerin
Clk  Clear  NC  NC  NC  NC  NC  NC  NC  GND
 OE  NC      NC /Q3 /Q2 /Q1 /Q0  NC  NC  VCC

  Q3 :=  Clear
       + /Q3 * /Q2 * /Q1 * /Q0
       +  Q3 *  Q0
       +  Q3 *  Q1
       +  Q3 *  Q2

  Q2 :=  Clear
       + /Q2 * /Q1 * /Q0
       +  Q2 *  Q0
       +  Q2 *  Q1

  Q1 :=  Clear
       + /Q1 * /Q0
       +  Q1 *  Q0

  Q0 :=  Clear
       + /Q0

FUNCTION TABLE
OE Clear Clk    /Q0 /Q1 /Q2 /Q3
-------------------------------
 L   H    C     L   L   L   L
 L   L    C     H   L   L   L
 L   L    C     L   H   L   L
 L   L    C     H   H   L   L
 L   L    C     L   L   H   L
 L   H    C     L   L   L   L
-------------------------------
```



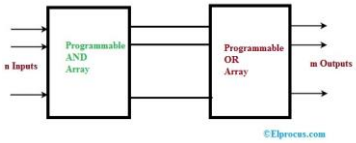
The programmable logic device (PLD)

- One kind of chip
- Used to implement the logic circuit
- It includes a set of logic circuit elements
- That can be modified in several ways.
- PLDs (different types)
  - SPLD-simple PLD (PLA & PAL)
  - CPLD-complex PLD
  - FPGAs-field programmable gate arrays.

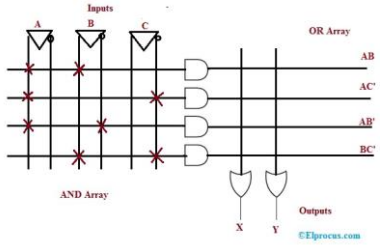
Programmable Array Logic



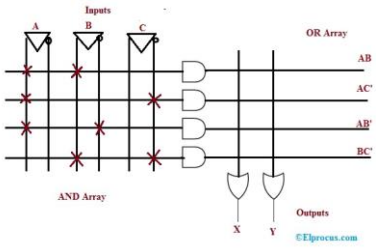
Programmable Logic Array



Design of Programmable Array Logic (PAL)

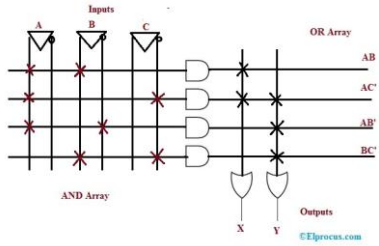


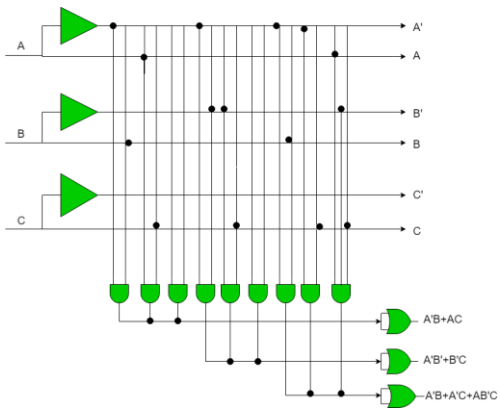
X =AB +AC' ???
Y= AB'+ B' ???

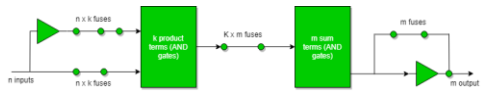


Design of Programmable Logic Array (PLA)

X = AB + AC'
Y = AB' +BC + AC'







- Field-Programmable Gate Array" or FPGA.
  - Intel (who acquired Altera)
  - Xilinx