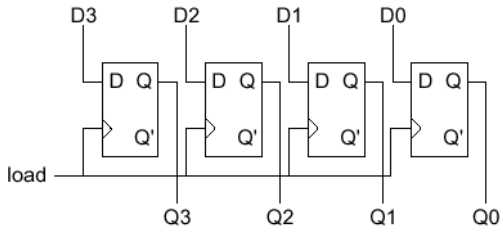
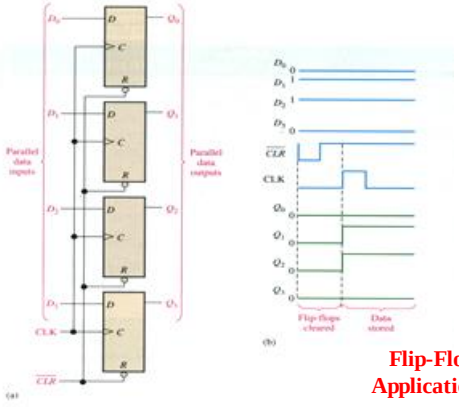
Dept. of Computer Science and Engineering
University of Rajshahi
www.ru.ac.bd

Dr. Shamim Ahmad

Flip-Flop Applications

Register



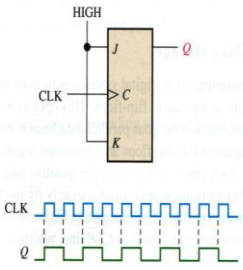


Flip-Flop Applications

Flip-Flop Applications

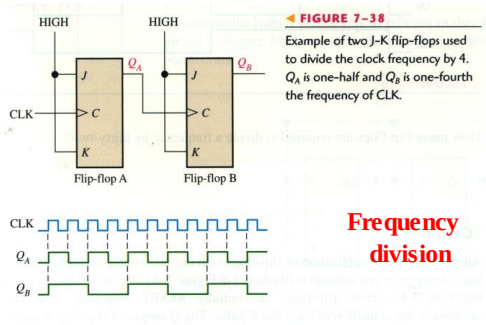
FIGURE 7–37

The J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.



Frequency division

Flip-Flop Applications

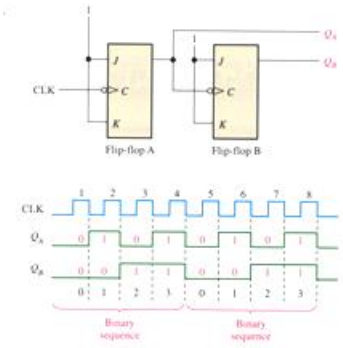


◀ FIGURE 7–38

Example of two J-K flip-flops used to divide the clock frequency by 4. Q_A is one-half and Q_B is one-fourth the frequency of CLK.

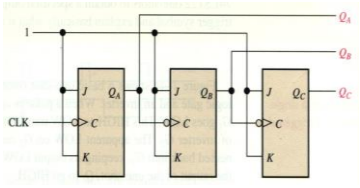
Frequency division

Flip-Flop Applications

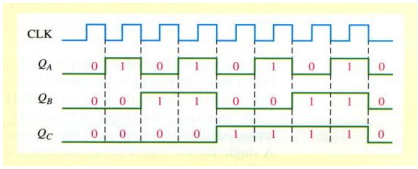


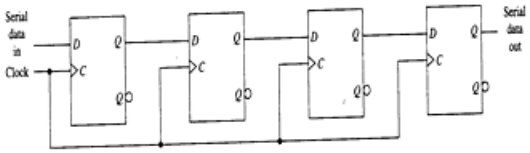
Counting

Flip-Flop Applications



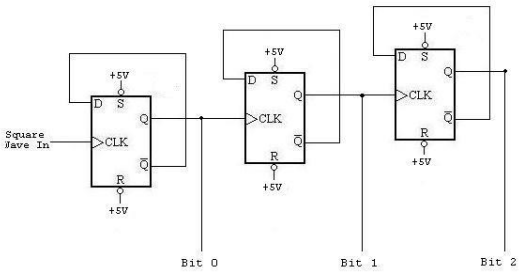
Counting



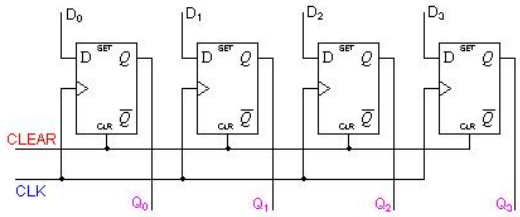


- Register is a group of Flip-Flops.
- It stores binary information 0 or 1.
- It is capable of moving data left or right with clock pulse.
- Registers are classified as

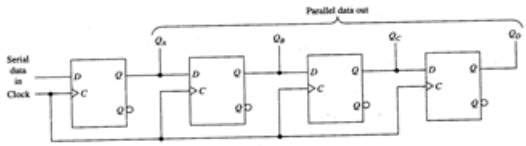
Shift Register

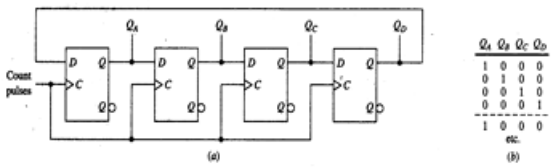


Shift Register

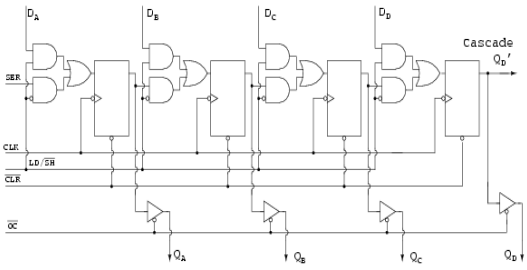


- Parallel-in Serial-Out
- Parallel-in parallel Out

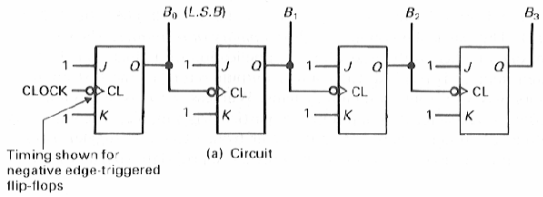


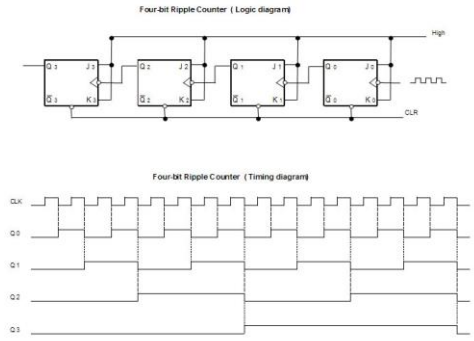


- The output of LSB FF is connected as D input to MSB FF.
- This is commonly called as Ring Counter or Circular Counter.
- The data is shifted to right with each clock pulse.
- This counter has four different states.
- This can be extended to any no. of bits.

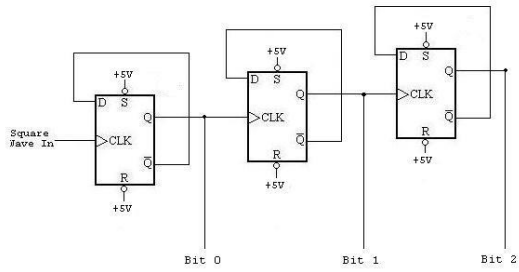


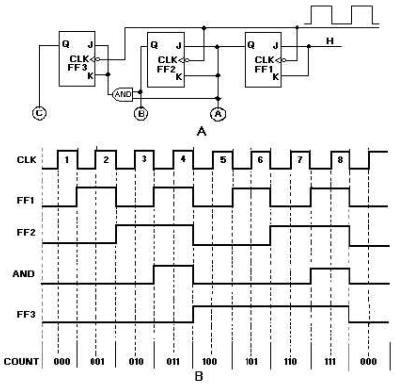
74LS395 parallel-in/ parallel-out shift register with tri-state output





Counter

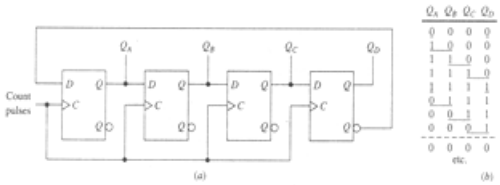




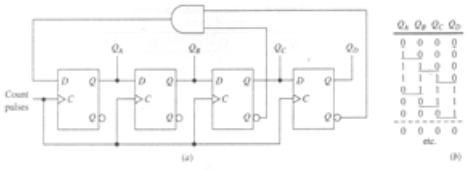
A

B

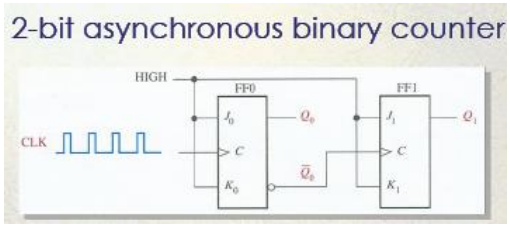
Twisted Ring Counter or Johnson Counter

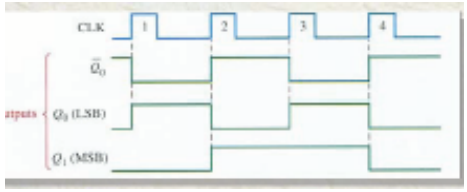


- The complement output of LSB FF is connected as D input to MSB FF.
- This is commonly called as Johnson Counter.
- The data is shifted to right with each clock pulse.
- This counter has eight different states.
- This can be extended to any no. of bits.

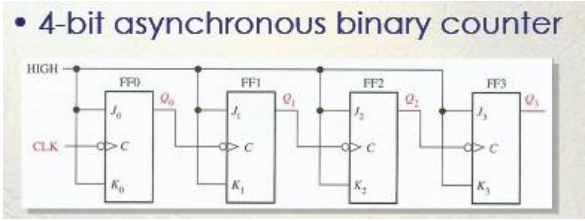


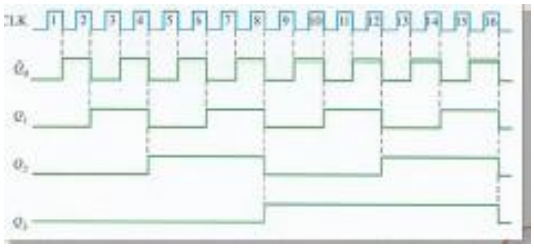
- The D input to MSB FF is
- The counter follows seven different states with application of clock input.
- By changing feedback different counters can be obtained.



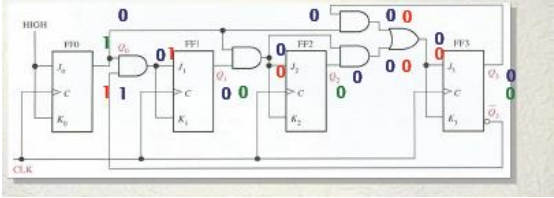


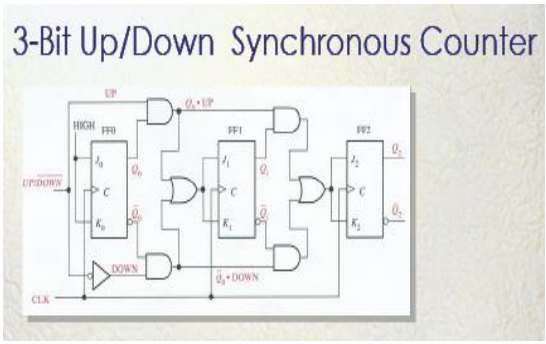
- 4-bit asynchronous binary counter

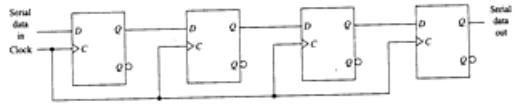




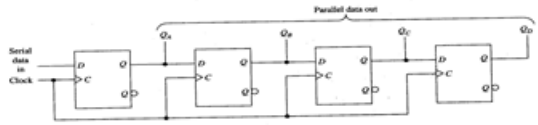
Synchronous BCD decade counter

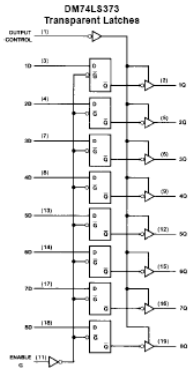




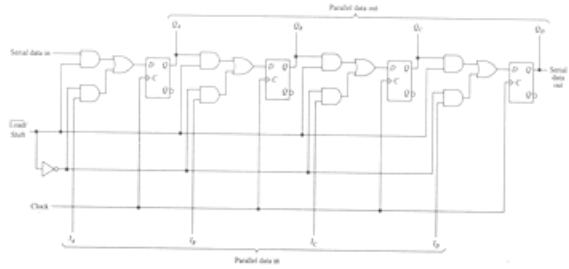


- Register is a group of Flip-Flops.
- It stores binary information 0 or 1.
- It is capable of moving data left or right with clock pulse.
- Registers are classified as





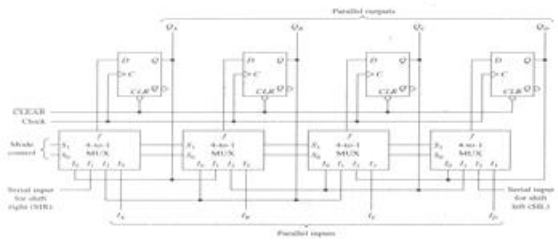
Parallel-in Unidirectional Shift Register



- **Parallel input data is applied at $I_A I_B I_C I_D$.**
- **Parallel output $Q_A Q_B Q_C Q_D$.**
- **Serial input data is applied to A FF.**
- **Serial output data is at output of D FF.**
- **L/Shift is common control input.**
- **L/S = 0, Loads parallel data into register.**
- **L/S = 1, shifts the data in one direction.**

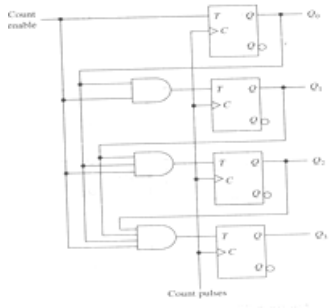
Select lines S_1	S_0	Register operation
0	0	Hold
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Universal Shift Register



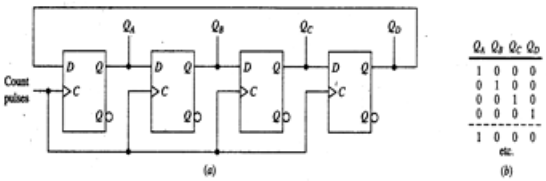
- Bidirectional Shifting.
- Parallel Input Loading.
- Serial-Input and Serial-Output.
- Parallel-Input and Serial-Output.
- Common Reset Input.
- 4:1 Multiplexer is used to select register operation.

Synchronous Binary Counter



- **The clock input is common to all Flip-Flops.**
- **The T input is function of the output of previous flip-flop.**
- **Extra combination circuit is required for flip-flop input.**

Counters Based on Shift Register



Q_A	Q_B	Q_C	Q_D
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0

etc.

(b)

- The output of LSB FF is connected as D input to MSB FF.
- This is commonly called as Ring Counter or Circular Counter.
- The data is shifted to right with each clock pulse.
- This counter has four different states.
- This can be extended to any no. of bits.