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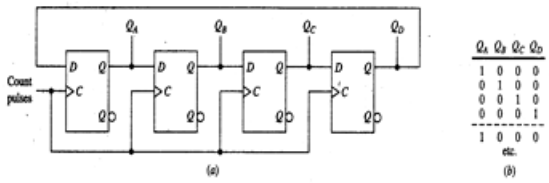
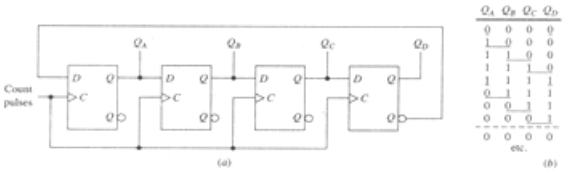
Counters Based on Shift Register



- The output of LSB FF is connected as D input to MSB FF.
- This is commonly called as Ring Counter or Circular Counter.
- The data is shifted to right with each clock pulse.
- This counter has four different states.
- This can be extended to any no. of bits.

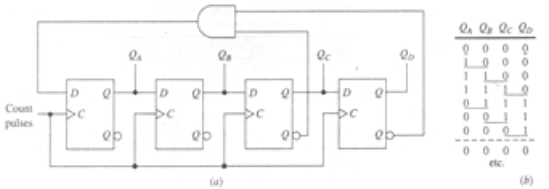
Twisted Ring Counter or Johnson Counter

Mod-8 Johnson Counter



- The complement output of LSB FF is connected as D input to MSB FF.
- This is commonly called as Johnson Counter.
- The data is shifted to right with each clock pulse.
- This counter has eight different states.
- This can be extended to any no. of bits.

Mod-7 Twisted Ring Counter



- The D input to MSB FF is
- The counter follows seven different states with application of clock input.
- By changing feedback different counters can be obtained.

Design Procedure for Synchronous Counter

- The clock input is common to all Flip-Flops.
- Any Flip-Flop can be used.
- For mod-n counter 0 to n-1 are counter states.
- The excitation table is written considering the present state and next state of counter.
- The flip-flop inputs are obtained from characteristic equation.
- By using flip-flops and logic gate the implementation of synchronous counter is obtained.

Difference between Asynchronous and Synchronous Counter

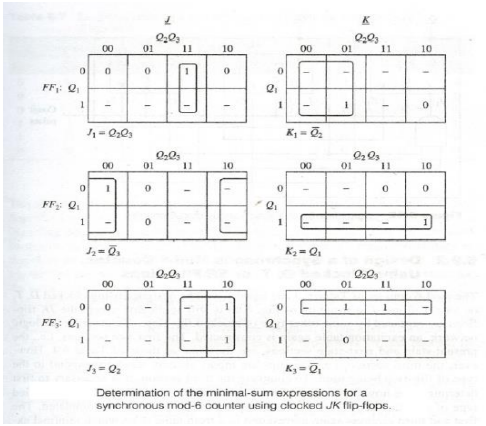
Asynchronous Counter	Synchronous Counter
1. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.	1. Clock input is common to all FF.
2. All Flip-Flops are toggle FF.	2. Any FF can be used.
3. Speed depends on no. of FF used for n bit .	3. Speed is independent of no. of FF used.
4. No extra Logic Gates are required. Cost is less.	4. Logic Gates are required based on design. Cost is more.

Design of Mod-6 Synchronous counter

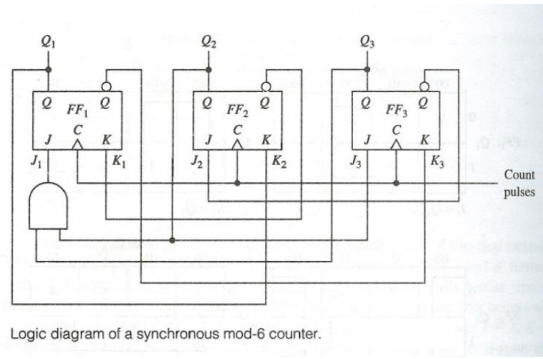
- The count sequence for Mod-6 counter is as follows:
- 000,010,011,110,101,001
- Excitation table is formed for given count sequence.
- Flip-flop inputs are derived from present state and next state.
- From K –map simplification the Flip-flop input equations are obtained.
- Logic diagram of Mod-6 counter is drawn by using JK-FF and logic gates.

Excitation table for a synchronous mod-6 counter using clocked *JK* flip-flops

Present state			Next state			Flip-flop inputs					
Q_1	Q_2	Q_3	Q_1^+	Q_2^+	Q_3^+	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0	0	1	0	0	–	1	–	0	–
0	1	0	0	1	1	0	–	–	0	1	–
0	1	1	1	1	0	1	–	–	0	–	1
1	1	0	1	0	1	–	0	–	1	1	–
1	0	1	0	0	1	–	1	0	–	–	0
0	0	1	0	0	0	0	–	0	–	–	1

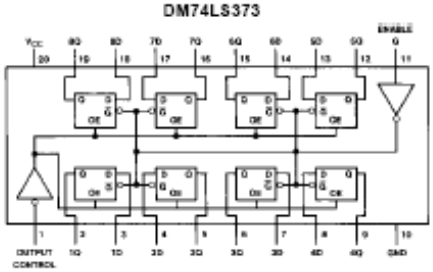


Determination of the minimal-sum expressions for a synchronous mod-6 counter using clocked JK flip-flops.



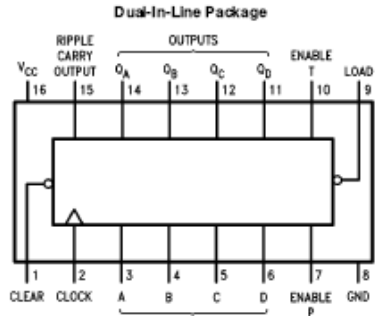
Logic diagram of a synchronous mod-6 counter.

DM74LS373

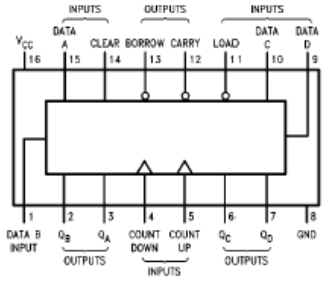


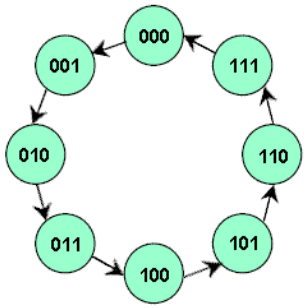
DM54161/DM74161/DM74163
Synchronous 4-Bit Counters

Dual-In-Line Package

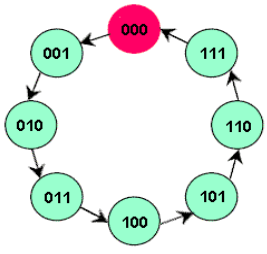


DM74LS193
Synchronous 4-Bit Binary Counter with Dual Clock





This example is taken from T. L. Floyd, *Digital Fundamentals*, Fourth Edition, Macmillan Publishing, 1990, p.395.

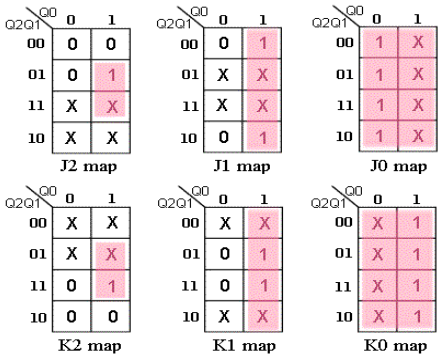


0

Clk

Present State $Q_2\ Q_1\ Q_0$	Next State $Q_2\ Q_1\ Q_0$
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0

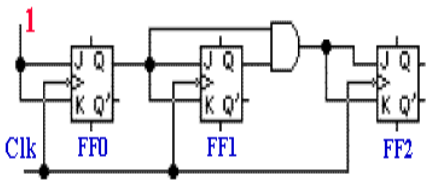
Output State Transitions		Flip-flop inputs		
Present State	Next State			
$Q_2\ Q_1\ Q_0$	$Q_2\ Q_1\ Q_0$	$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

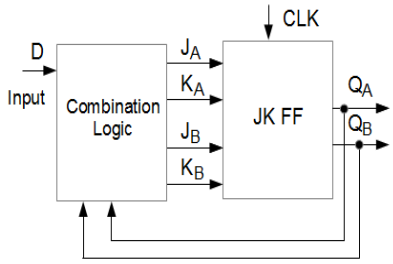


$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_1 * Q_0$




CLK
D
Input
Combination Logic
J_A
K_A
J_B
K_B
JK FF
Q_A
Q_B