# Overview

- Why VLSI?
- Moore's Law.
- The VLSI design process.


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# Integrated Circuits (IC)

| Name | Signification | Year | Transistors number | Logic gates number |
|---|---|---|---|---|
| SSI | small-scale integration | 1964 | 1 to 10 | 1 to 12 |
| MSI | medium-scale integration | 1968 | 10 to 500 | 13 to 99 |
| LSI | large-scale integration | 1971 | 500 to 20,000 | 100 to 9,999 |
| VLSI | very large-scale integration | 1980 | 20,000 to 1,000,000 | 10,000 to 99,999 |
| ULSI | ultra-large-scale integration | 1984 | 1,000,000 and more | 100,000 and more |


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# VLSI

- Acronym of VLSI
  - Very-Large-Scale Integration
- A VLSI contains more than a million or so switching devices or logic gates
- Early in the first decade of the 21st century, the actual number of transistors has exceeded 100 million
- A piece of silicon (a chip) is typically about 1 centimeter on a side


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# Why VLSI?

- Integration improves the design:
  - lower parasitics = higher speed;
  - lower power;
  - physically smaller.
- Integration reduces manufacturing cost- (almost) no manual assembly.


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## VLSI and you

- Microprocessors:
  - personal computers;
  - microcontrollers.
- DRAM/SRAM.
- Special-purpose processors.


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## VLSI Design Styles

- Full Custom
- Application-Specific Integrated Circuit (ASIC)
- Programmable Logic (PLD, FPGA)
- System-on-a-Chip


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## Full Custom Design

- Each circuit element carefully “handcrafted”
- Huge design effort
- High Design & NRE Costs / Low Unit Cost
- High Performance
- Typically used for high-volume applications


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## ASIC

- Constrained design using pre-designed (and sometimes pre-manufactured) components
- Also called semi-custom design
- CAD tools greatly reduce design effort
- Low Design Cost / High NRE Cost / Med. Unit Cost
- Medium Performance


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## Programmable Logic (FPGA)

- Pre-manufactured components with programmable interconnect
- CAD tools greatly reduce design effort
- Low Design Cost / Low NRE Cost / High Unit Cost
- Lower Performance


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## System-on-chip (SOC)

- Idea: combine several large blocks
  - Predesigned custom cores (e.g., microcontroller) - "intellectual property" (IP)
  - ASIC logic for special-purpose hardware
  - Programmable Logic (PLD, FPGA)
  - Analog
- Open issues
  - Keeping design cost low
  - Verifying correctness of design


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## Moore's Law

- Gordon Moore: co-founder of Intel.
- Predicted that number of transistors per chip would grow exponentially (double every 18 months).
- Exponential improvement in technology is a natural trend: steam engines, dynamos, automobiles.


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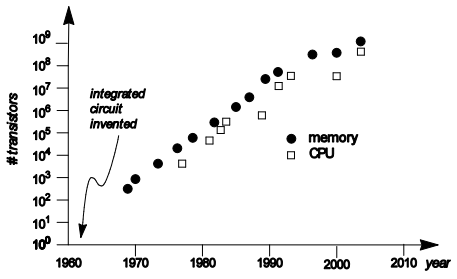
## Moore's Law plot





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## Choice of technology

- Two distinct types of technology are fabricated in silicon based upon
  - BJT (Bipolar Junction Transistor)
  - MOS (Metallic Oxide Semiconductor)
- Since processing of these technologies is very different, it is impractical to mix them up within a chip


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## Choice of MOS and BJT

- MOS logic occupies much smaller area of silicon than the equivalent BJT logic
- MOS technology has a much higher potential packing density
- A MOS logic circuit requires appreciably less current and hence less power than its bipolar counter part
- However, bipolar circuits operate faster than MOS circuits
- Even so, the speed-power product for MOS logic compares favorably with that of BJT logic


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## Terminology

- Manufacturing node: technology at a particular channel length.
- Deep submicron technology: 250-100 nm.
- Nanometer technology: 100 nm and below.


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## Design metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

## Cost factors in ICs

- For large-volume ICs:
  - packaging is largest cost;
  - testing is second-largest cost.
- For low-volume ICs, design costs may swamp all manufacturing costs.


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## Cost of design

- Design cost can be significant: $20 million for a large ASIC, $500 million for a large CPU.
- Cost elements:
  - Architects, logic designers, etc.
  - CAD tools.
  - Computers the CAD tools run on.


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## Reliability

- Nanometer technologies require attention to reliability.
- Design-for-manufacturing (DFM) and design-for-yield (DFY) techniques adjust the design to improve yield.
- Circuit and architecture techniques can compensate for unreliable components.


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## The VLSI design process

- May be part of larger product design.
- Major levels of abstraction:
  - specification;
  - architecture;
  - logic design;
  - circuit design;
  - layout.


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## Challenges in VLSI design

- Multiple levels of abstraction: transistors to CPUs.
- Multiple and conflicting constraints: low cost and high performance are often at odds.
- Short design time: Late products are often irrelevant.


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## Integrated Circuit Design Techniques

- Hierarchical design
- Design abstraction


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## Hierarchical Design

- Divide-and-conquer: limit the number of components you deal with at any one time.
- Group several components into larger components:
  - transistors form gates;
  - gates form functional units;
  - functional units form processing elements;
  - etc.


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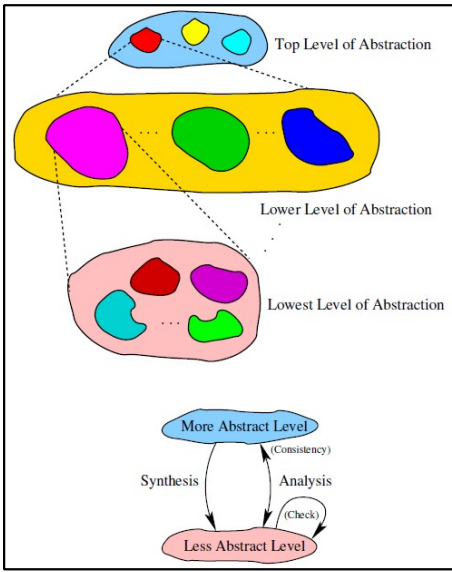
## Hierarchical Design…….

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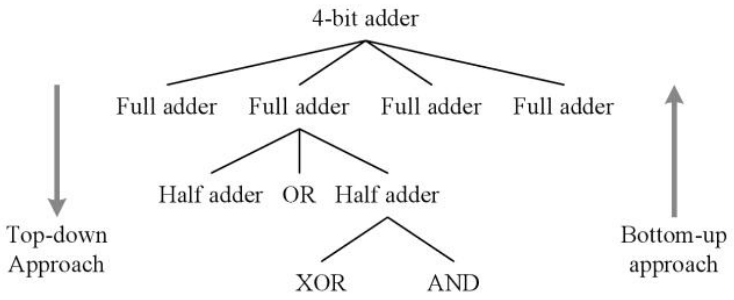
## Concept of Hierarchical design




Concept of Hierarchical Design

## Top-down vs. bottom-up design

- Top-down design adds functional detail.
  - Create lower levels of abstraction from upper levels.
- Bottom-up design creates abstractions from low-level behavior.
- Good design needs both top-down and bottom-up efforts.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## Design abstraction….

- Hardware design requires multiple-level of design abstraction to manage the design process and ensure that they meet major design goals (speed, power consumption etc.)


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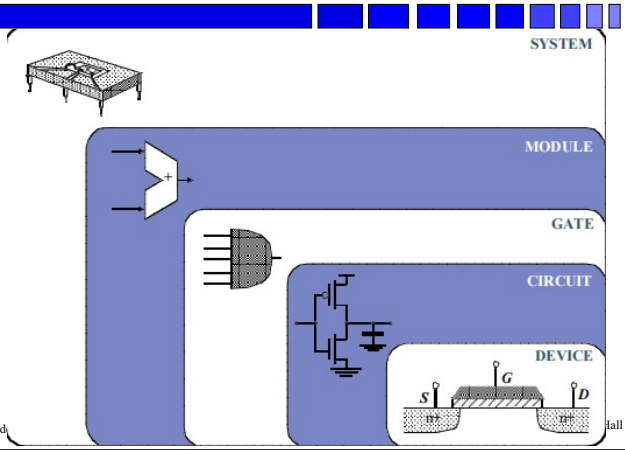
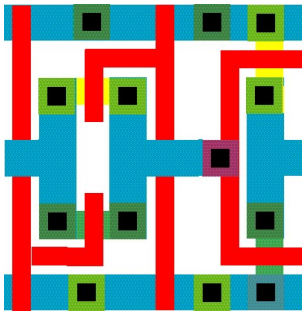
## Design abstraction levels



## Example: Layout and its abstractions

- Layout for dynamic latch:

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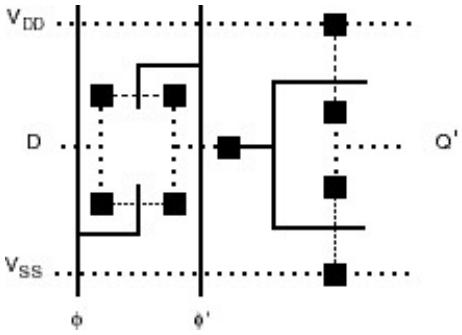
## Stick diagram





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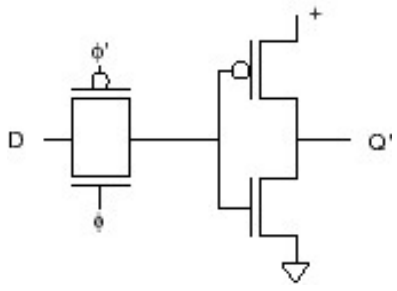
## Transistor schematic





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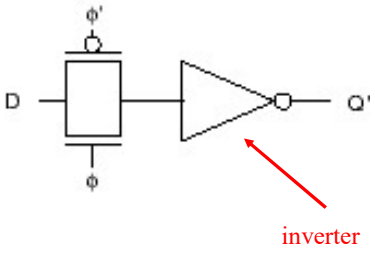
## Mixed schematic





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## Levels of abstraction

- Specification: function, cost, etc.
- Architecture: large blocks.
- Logic: gates + registers.
- Circuits: transistor sizes for speed, power.
- Layout: determines parasitics.


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## Design validation

- Must check at every step that errors haven't been introduced-the longer an error remains, the more expensive it becomes to remove it.
- Forward checking: compare results of less- and more-abstract stages.
- Back annotation: copy performance numbers to earlier stages.


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## Manufacturing test

- Not the same as design validation: just because the design is right doesn't mean that every chip coming off the line will be right.
- Must quickly check whether manufacturing defects destroy function of chip.
- Must also speed-grade.


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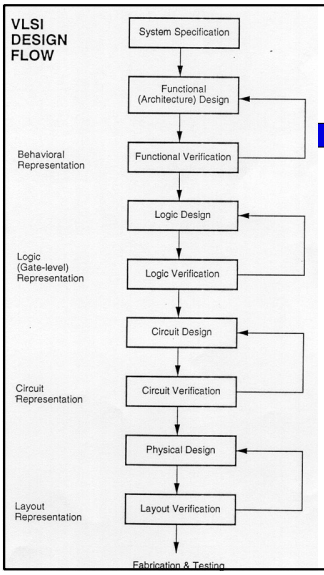
## Design flow

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