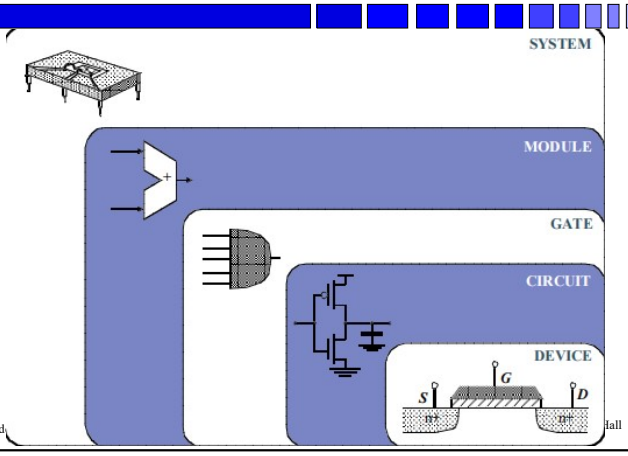
Design abstraction & Wafer preparation

Design abstraction….

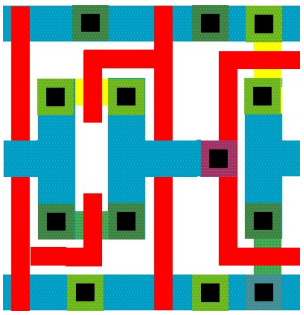
- Hardware design requires multiple-level of design abstraction to manage the design process and ensure that they meet major design goals (speed, power consumption etc.)

Design abstraction levels

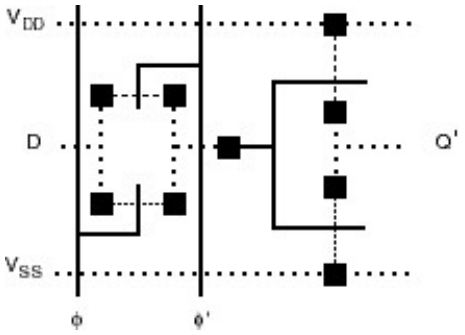


Example: Layout and its abstractions

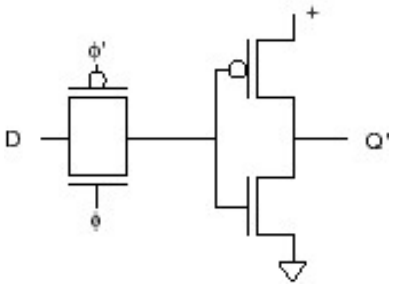
- Layout for dynamic latch:



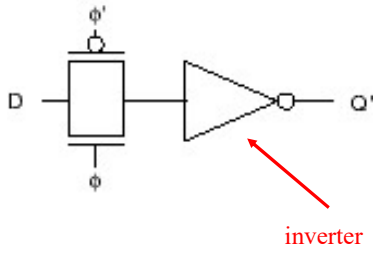
Stick diagram



Transistor schematic



Mixed schematic



Levels of abstraction

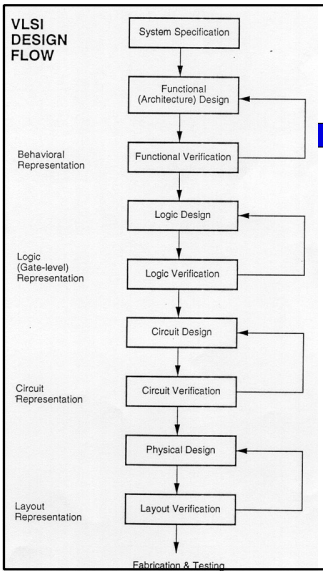
- Specification: function, cost, etc.
- Architecture: large blocks.
- Logic: gates + registers.
- Circuits: transistor sizes for speed, power.
- Layout: determines parasitics.

Design validation

- Must check at every step that errors haven't been introduced-the longer an error remains, the more expensive it becomes to remove it.
- Forward checking: compare results of less- and more-abstract stages.
- Back annotation: copy performance numbers to earlier stages.

Manufacturing test

- Not the same as design validation: just because the design is right doesn't mean that every chip coming off the line will be right.
- Must quickly check whether manufacturing defects destroy function of chip.
- Must also speed-grade.



Design flow

Wafer Preparation

Silicon Wafer Preparation..

Silicon wafer preparation stages

Manufacture of IC grade silicon wafers proceeds in four stages.

- Conversion of sand (ore) to a high-purity gas
- Conversion of gas to polysilicon silicon
- Conversion of polysilicon silicon to a single crystalline, doped crystal ingot
- Preparation of wafers from the crystal ingot

Conversion of ore to a high-purity gas

First, metallurgical-grade silicon (MGS) with purity up to 99% is produced in a furnace. The silica is reduced (oxygen removed) through a reaction with carbon in the form of coal, charcoal and heating to 1500-2000C in an electrode arc furnace.

$$C + SiO_2 \rightarrow Si(liquid) + SiO(gas) + CO\ (gas)$$

The next process step is to pulverize the MGS mechanically and react it with anhydrous hydrogen chloride to form *trichlorosilane* ($SiHCl_3$) according to the reaction:

$$Si(solid) + 3HCl(gas) \rightarrow SiHCl_3\ (gas) + H_2\ (gas) + heat$$

Conversion of gas to polysilicon silicon

Electronic Grade of Silicon (EGS) is prepared from the purified $SiHCl_3$. The chemical reaction is a hydrogen reduction of trichlorosilane(TCS).

$$\mathbf{2SiHCl_3(gas) + 2H_2(gas) \rightarrow 2Si(solid) + 6HCl(gas)}$$

Crystal Growth

Semiconductor wafers are cut from large crystals of the semiconducting material. These crystals, also called *ingots*, are grown from chunks of the intrinsic material, which have a polycrystalline structure and are undoped. The process of converting the polycrystalline chunks to a large crystal of single-crystal structure, with the correct orientation and the proper amount of N- or P-type, is called ***crystal growing***.

Three different methods are used to grow crystals:

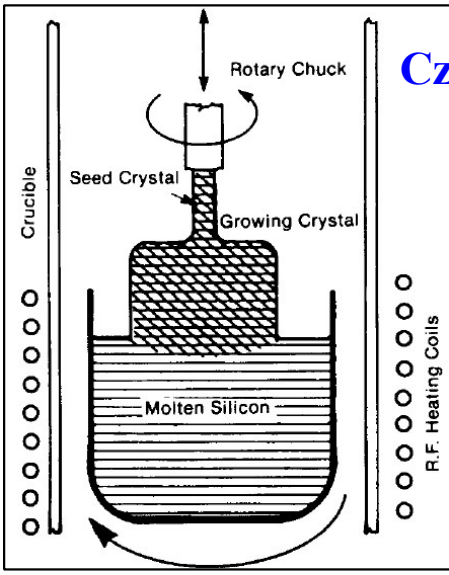
- ***Czochralski (CZ)***,
- ***Liquid Encapsulated Czochralski***, &
- ***Float Zone (FZ)***

Crystal Growth: Czochralski (CZ) method

The majority of silicon crystals are grown by the CZ method (Fig. 3.8). The equipment consists of a quartz (silica) crucible that is heated by surrounding coils that carry radio frequency (RF) waves or by electric heaters. The crucible is loaded with chunks of polycrystalline of the semiconductor material and small amounts of dopant. The dopant material is selected to create either an N-type or P-type crystal. First, the poly and dopants are heated to the liquid state at 1415°C (Fig. 3.9).

Next, a seed crystal is positioned to just touch the surface of the liquid material (called the *melt*). The seed is a small crystal that has the same crystal orientation required in the finished crystal. Seeds can be

Czochralski (CZ) method



Zo-cra-liski

Drawback to the CZ method

- The inclusion of oxygen from the crucible into the crystal.
  - For some devices, higher levels of oxygen are intolerable. For these special cases, the crystal might be grown by the float zone technique, which produces a lower oxygen content crystal.
- This limits the resistivity to ~20Ωcm, while intrinsic Si is 230kΩcm.

Float-zone Technique: overview

- These crystals are more expensive and have very low oxygen and carbon.
- Carrier concentrations down to 10^{11} atoms/cm^3 is possible to achieve.
- It is far less common, and is reserved for situations where oxygen and carbon impurities cannot be tolerated.
- Float-zone does not allow as large Si wafers as CZ does (200mm and 300mm) and radial distribution of dopant in FZ wafer is not as uniform as in CZ wafer.
- It is good for solar cells, power electronic devices (thyristors and rectifiers) that use the entire volume of the wafer not just a thin surface layer, etc.

Float Zone (FZ)

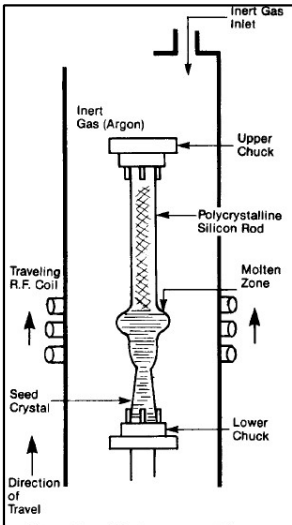


Figure 3.11 Float zone crystal-growing system.

* Float zone (FZ) crystal growth requires a bar of the polysilicon. The seed is fused to one end of the bar and the assemblage placed in the crystal grower.
* Crystal growing starts when an RF coil heats the interface region of the bar and seed.
* The coil is then moved along the axis of the bar, heating it to the liquid point a small section at a time.
* Within each molten region, the atoms align to the orientation started at the seed end.