Wafer Fabrication

Basic steps of IC Fabrication

Followings are the basic steps used in an infinite number of sequences and variations to produce specific microchips.

- *Layering,*
- *Patterning,*
- *Doping, and*
- *Heat treatment*

1-Layering

Layering

- ***Grown*** (*Oxidation(**SiO_2**), Nitridation (**Si_3N_4**)*)
- ***Deposited*** (*CVD, Sputtering, Evaporation, Electroplating*)

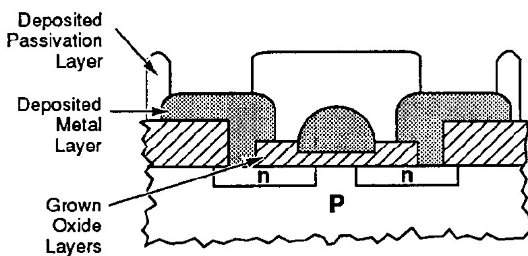


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

2-Patterning

- The patterning process is known by the names photomasking, masking, photolithography, and microlithography.
- Patterning is the series of steps that results in the removal of selected portions of the added surface layers

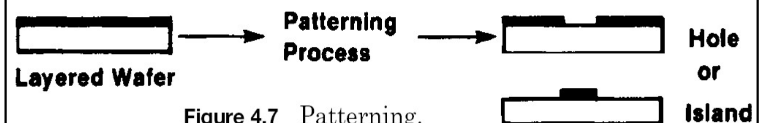


Figure 4.7 Patterning.

3-Doping

- Doping is the process that puts specific amounts of electrically active dopants in the wafer surface through openings in the surface layers
  - *thermal diffusion* and
  - *ion implantation*

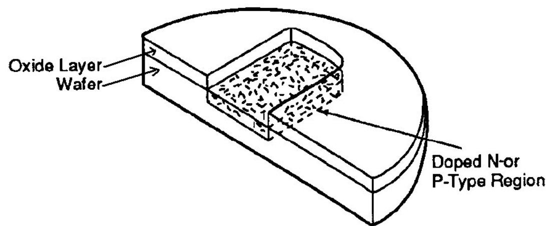


Figure 4.9 Formation of N- or P-type region in wafer surface.

4-Heat treatment

- Heat treatments are the operations in which the wafer is simply heated and cooled to achieve specific results

Operation	Heat treatment
Patterning	Soft bake Hard bake Post exposure bake (develop)
Doping	Post ion implant anneal
Layering	Post metal deposition and patterning anneal

Figure 4.10 Table of major heat treatments

Fabrication processes

- IC built on silicon substrate:
  - some structures diffused into substrate;
  - other structures built on top of substrate.
- Substrate regions are doped with n-type and p-type impurities. (n+ = heavily doped)
- Wires made of polycrystalline silicon (poly), multiple layers of aluminum (metal).
- Silicon dioxide (SiO_2) is insulator.

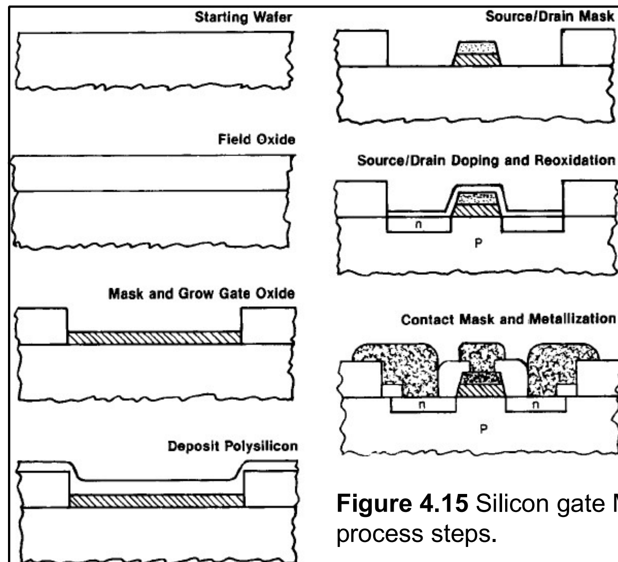
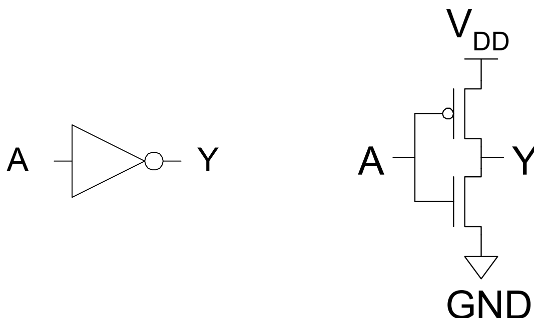


Figure 4.15 Silicon gate MOS process steps.

Step 1: Layering Operation. The building starts with an oxidation of the wafer surface to form a thin protective layer and to serve as a doping barrier. This silicon dioxide layer is called the *field oxide*.
Step 2: Patterning Operation. The patterning process leaves a hole in the field oxide that defines the location of the source, gate, and drain areas of the transistor.
Step 3: Layering Operation. Next, the wafer goes to an silicon dioxide oxidation operation. A thin oxide is grown on the exposed silicon. It will service as the gate oxide.
Step 4: Layering Operation. In step 4, another layering operation is used to deposit a layer of polycrystalline (poly) silicon. This layer will also become part of the gate structure.
Step 5: Patterning Operation. Two openings are patterned in the oxide/polysilicon layer to define the source and drain areas of the transistor.
Step 6: Doping Operation. A doping operation is used to create an N-type pocket in the source and drain areas.
Step 7: Layering Operation. Another oxidation/layering process is used to grow a layer of silicon dioxide over the source/drain areas.

Step 8: Patterning Operation. Holes, called contact holes, are patterned in the source, gate, and drain areas.
Step 9: Layering Operation. A thin layer of conducting metal, usually an aluminum alloy, is deposited over the entire wafer.
Step 10: Patterning Operation. After deposition, the wafer goes back to the patterning area where portions of the metallization layer are removed from the chip area and the scribe lines. The remaining portions connect all the parts of the surface components to each other in the exact pattern required by the circuit design.
Step 11: Heat Treatment Operation. Following the metal patterning step, the wafer goes through a heating process in a nitrogen gas atmosphere. The purpose of the step is to “alloy” the metal to the exposed source and drain regions and the gate region to ensure good electrical contact.
Step 12: Layering Operation. The final layer of this device is a protective layer known variously as a *scratch* or *passivation layer*. Its purpose is to protect the components on the chip surface during the testing and packaging processes, and during use.
Step 13: Patterning Operation. The last step in the sequence is a patterning process that removes portions of the scratch protection layer over the metallization terminal pads on the periphery of the chip. This step is known as the *pad mask*.

CMOS Inverter



CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

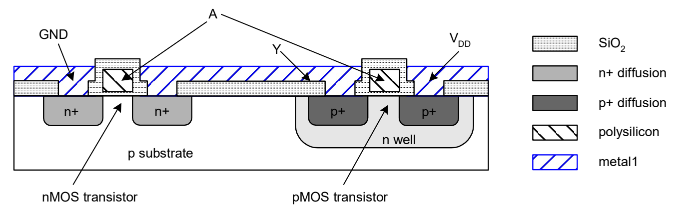
Types of CMOS fabrication

- N-TUB Fabrication
- P-TUB Fabrication
- Twin-TUB Fabrication

Advantages of Fabrication using Tub/Well

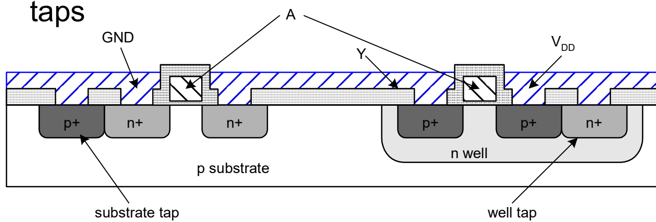
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



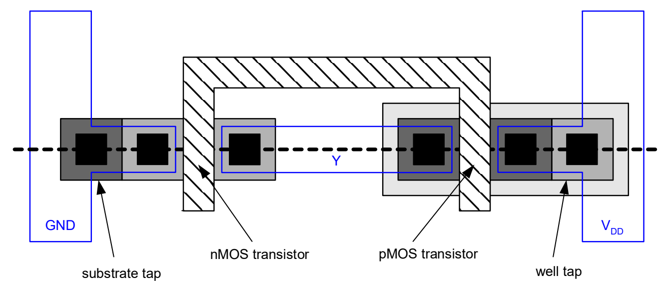
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



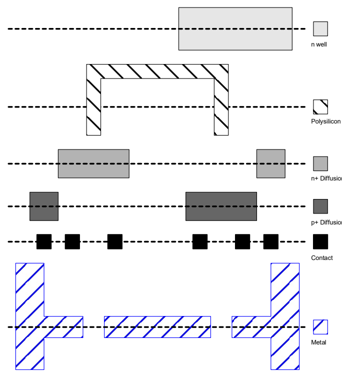
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



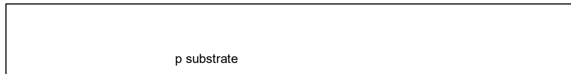
Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



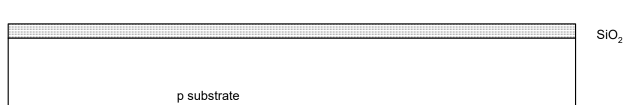
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2



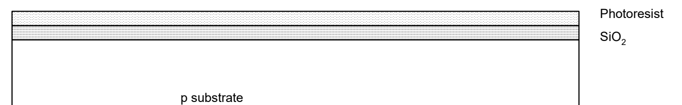
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



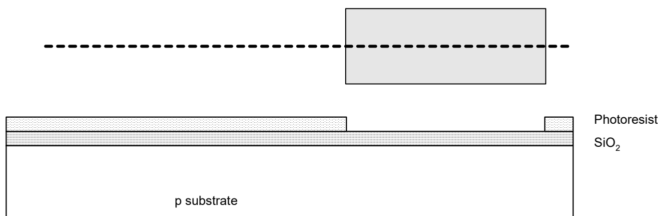
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



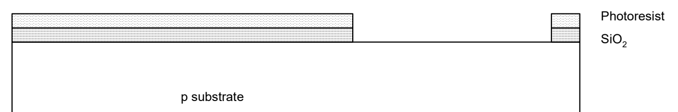
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



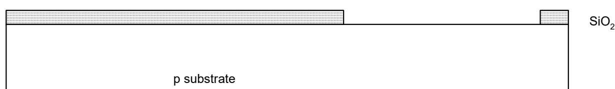
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



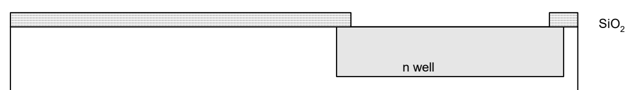
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

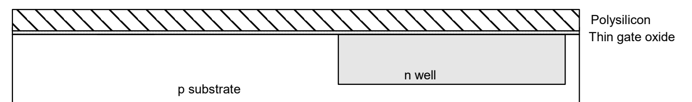


Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

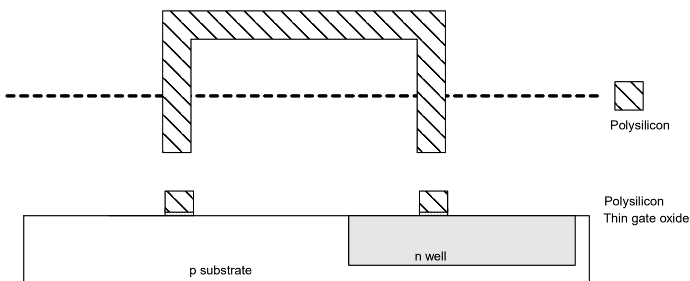
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



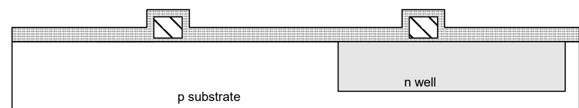
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



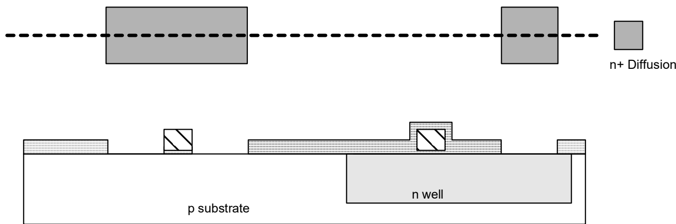
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



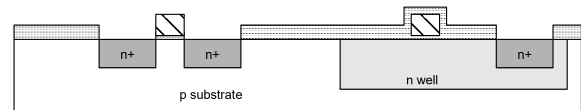
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



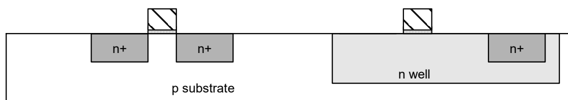
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



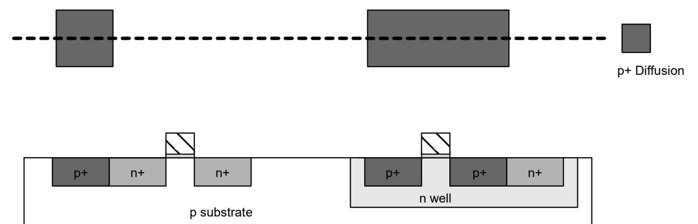
N-diffusion cont.

- Strip off oxide to complete patterning step



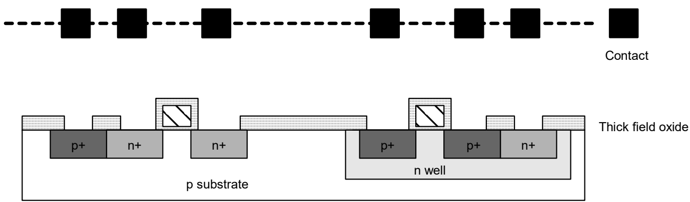
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



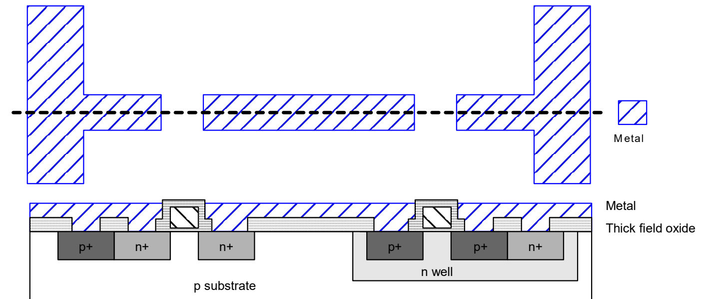
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

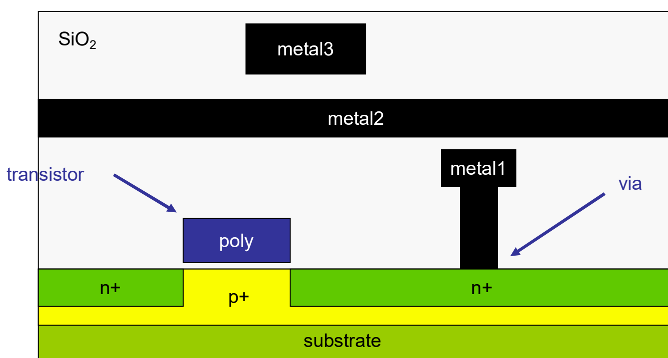


Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



Simple cross section



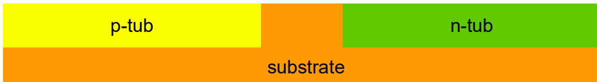
Photolithography

Mask patterns are put on wafer using photo-sensitive material:

Process steps

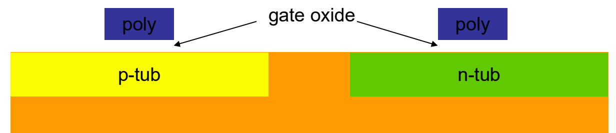
- First place tubs (wells) to provide properly-doped substrate for n-type, p-type transistors.

a twin-tub process:



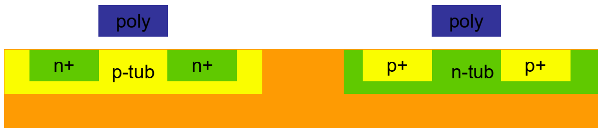
Process steps, cont'd.

Pattern polysilicon before diffusion regions:



Process steps, cont'd

Add diffusions, performing self-masking:



Process steps, cont'd

Start adding metal layers: