VLSI Design Rules

Why we need design rules

- Masks are tooling for manufacturing.
- Manufacturing processes have inherent limitations in accuracy.
- Design rules specify geometry of masks which will provide reasonable yields.
- Design rules are determined by experience.

Manufacturing problems

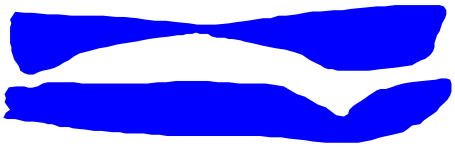
- Photoresist shrinkage, tearing.
- Variations in material deposition.
- Variations in temperature.
- Variations in oxide thickness.
- Impurities.
- Variations between lots.
- Variations across a wafer.

Transistor problems

- Varaiations in threshold voltage:
  - oxide thickness;
  - ion implanatation;
  - poly variations.
- Changes in source/drain diffusion overlap.
- Variations in substrate.

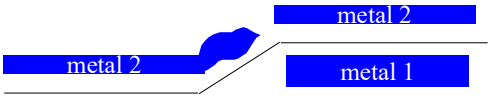
Wiring problems

- Diffusion: changes in doping -> variations in resistance, capacitance.
- Poly, metal: variations in height, width -> variations in resistance, capacitance.
- Shorts and opens:



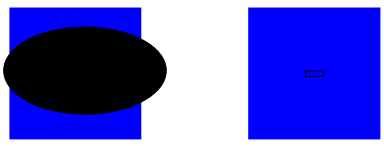
Oxide problems

- Variations in height.
- Lack of planarity -> step coverage.



Via problems

- Via may not be cut all the way through.
- Undesize via has too much resistance.
- Via may be too large and create short.



MOSIS SCMOS design rules

- Designed to scale across a wide range of technologies.
- Designed to support multiple vendors.
- Designed for educational use.

λ and design rules

- λ is the size of a minimum feature.
- Specifying λ particularizes the scalable rules.
- Parasitics are generally not specified in λ units.

Design Rules

- Typical rules:
  - Minumum size
  - Minimum spacing
  - Alignment / overlap
  - Composition
  - Negative features

Types of Design Rules

- Scalable Design Rules (e.g. SCMOS)
  - Based on scalable "coarse grid" - λ (lambda)
  - Idea: reduce λ value for each new process, but keep rules the same
    - » Key advantage: portable layout
    - » Key disadvantage: not everything scales the same
  - Not used in "real life"
- Absolute Design Rules
  - Based on absolute distances (e.g. 0.75μm)
  - Tuned to a specific process (details usually proprietary)
  - Complex, especially for deep submicron
  - Layouts not portable

SCMOS Design Rules

- Intended to be Scalable
  - Original rules: SCMOS
  - Submicron: SCMOS-SUBM
  - Deep Submicron: SCMOS-DEEP
- Pictorial Summary: Book Fig. 2-24, p. 27
- Authoritative Reference: www.mosis.org

SCMOS Design Rule Summary

- Line size and spacing:
  - metal1: Minimum width=3λ, Minimum Spacing=3λ
  - metal2: Minimum width=3λ, Minimum Spacing=4λ
  - poly: Minimum width= 2λ, Minimum Spacing=2λ
  - ndiff/pdiff: Minimum width= 3λ, Minimum Spacing=3λ, minimum ndiff/pdiff seperation=10λ
  - wells: minimum width=10λ, min distance form well edge to source/drain=5λ
- Transistors:
  - Min width=3λ
  - Min length=2λ

SCMOS Design Rule Summary

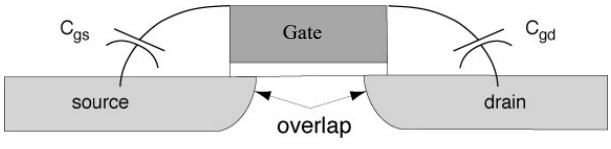
- Contacts (Vias)
  - Cut size: exactly 2λ X 2λ
  - Cut separation: minimum 2λ
  - Overlap: min 1λ in all directions
  - Magic approach: Symbolic contact layer min. size 4λ X 4λ
  - Contacts cannot stack (i.e., metal2/metal1/poly)
- Other rules
  - cut to poly must be 3λ from other poly
  - cut to diff must be 3λ from other diff
  - metal2/metal1 contact cannot be directly over poly
  - negative features must be at least 2λ in size
  - CMP Density rules (AMI/HP subm): 15% Poly, 30% Metal

MOS Parasitics

- Transistor
- Wire

Basic transistor parasitics

1. Gate to substrate, also gate to source/drain.
2. Source/drain capacitance, resistance.



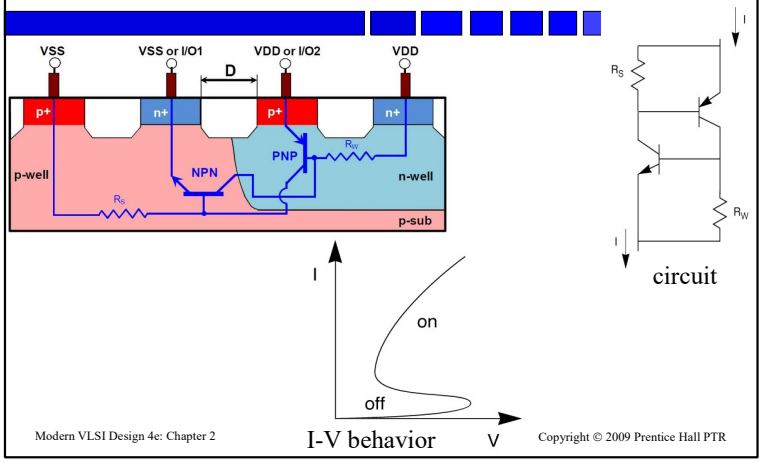
Basic transistor parasitics, cont'd

3. Gate capacitance C_g. Determined by active area.
4. Source/drain overlap capacitances C_{gs}, C_{gd}. Determined by source/gate and drain/gate overlaps. Independent of transistor L.
   - $C_{gs} = C_{ol}$ W
5. Gate/bulk overlap capacitance.

Latch-up

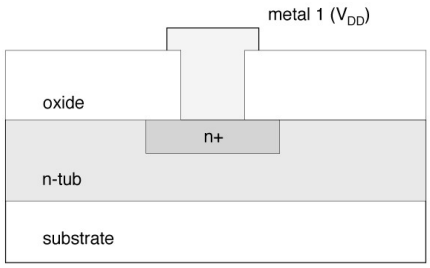
- CMOS ICs have parastic silicon-controlled rectifiers (SCRs).
- When powered up, SCRs can turn on, creating low-resistance path from power to ground. Current can destroy chip.
- Early CMOS problem. Can be solved with proper circuit/layout structures.

6. Parasitic SCR



Solution to latch-up

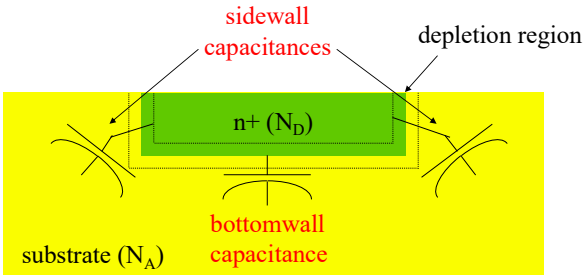
Use tub ties to connect tub to power rail. Use enough to create low-voltage connection.



Wire Parasitics

Diffusion wire capacitance

- Capacitances formed by p-n junctions:

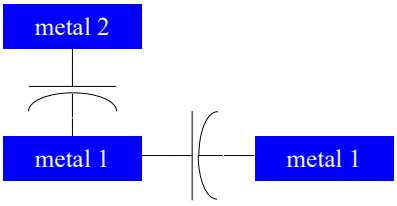


Depletion region capacitance

- Zero-bias depletion capacitance:
  - $C_{j0} = \varepsilon_{si}/x_d$.
- Depletion region width:
  - $x_{d0} = \text{sqrt}[(1/N_A + 1/N_D)2\varepsilon_{si}V_{bi}/q]$.
- Junction capacitance is function of voltage across junction:
  - $C_j(V_r) = C_{j0}/\text{sqrt}(1 + V_r/V_{bi})$

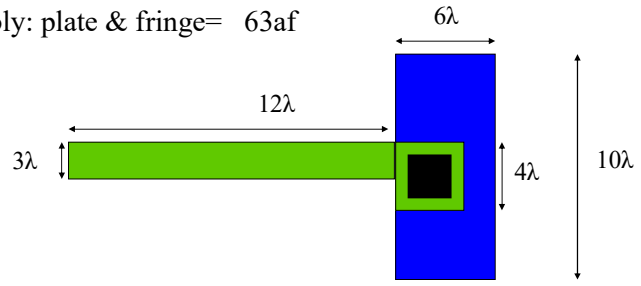
Metal coupling capacitances

- Can couple to adjacent wires on same layer, wires on above/below layers:



Example: parasitic capacitance measurement

- n-diffusion: bottom wall=940 aF/um², sidewall=200 aF/um.
- metal: plate=36 aF, fringe=54 aF.
- Poly: plate & fringe= 63af



N-diffusion layer capacitance calculation

- Bottom wall capacitance
  - Area of n-diffusion layer:
  - $3x12x\lambda^2 + 4x4\lambda^2 = 36\lambda^2 + 16\lambda^2 = 52\lambda^2 = 52(.09\mu m)^2 = 0.4212\mu m^2$
  - Bottom wall capacitance : 0.4212x940aF= 0.39fF
- Side wall capacitance:
  - Perimeter of side wall (counter clockwise)

$$0.27\mu m + 1.08\mu m + 0.09\mu m + 0.36\mu m + 0.36\mu m + 1.44\mu m = 3.6\mu m$$

  - Side wall capacitance: 3.6x200af = 0.72fF
- Total n-diffusion capacitance: 0.42 + 0.72 = **1.11fF**

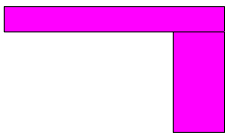
Typical parameters for 180 nm process.

p-type transconductance	k'_p	$-30\mu A/V^2$
n-type threshold voltage	V_{tn}	0.5V
p-type threshold voltage	V_{tp}	-0.5V
n-diffusion bottomwall capacitance	$C_{ndiff,bot}$	$940aF/\mu m^2$
n-diffusion sidewall capacitance	$C_{ndiff,side}$	$200aF/\mu m$
p-diffusion bottomwall capacitance	$C_{pdiff,bot}$	$1000aF/\mu m^2$
p-diffusion sidewall capacitance	$C_{pdiff,side}$	$200aF/\mu m$
n-type source/drain resistivity	R_{ndiff}	$7\Omega/\square$
p-type source/drain resistivity	R_{pdiff}	$7\Omega/\square$
poly-substrate plate capacitance	$C_{poly,plate}$	$63aF/\mu m^2$
poly-substrate fringe capacitance	$C_{poly,fringe}$	$63aF/\mu m$

poly resistivity	R_{poly}	$8\Omega/\square$
metal 1-substrate plate capacitance	$C_{metal1,plate}$	$36aF/\mu m^2$
metal 1-substrate fringe capacitance	$C_{metal1,fringe}$	$54aF/\mu m$
metal 2-substrate capacitance	$C_{metal2,plate}$	$36aF/\mu m^2$
metal 2-substrate fringe capacitance	$C_{metal2,fringe}$	$51aF/\mu m$
metal 3-substrate capacitance	$C_{metal3,plate}$	$37aF/\mu m^2$
metal 3-substrate fringe capacitance	$C_{metal3,fringe}$	$54aF/\mu m$
metal 1 resistivity	R_{metal1}	$0.08\Omega/\square$
metal 2 resistivity	R_{metal2}	$0.08\Omega/\square$
metal 3 resistivity	R_{metal3}	$0.03\Omega/\square$
metal current limit	$I_{m,max}$	$1mA/\mu m$

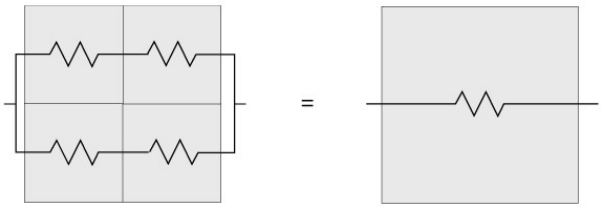
- What will be the metal wire capacitance?

Parasitic Resistance Calculation



Wire resistance

- Resistance of any size square is constant:

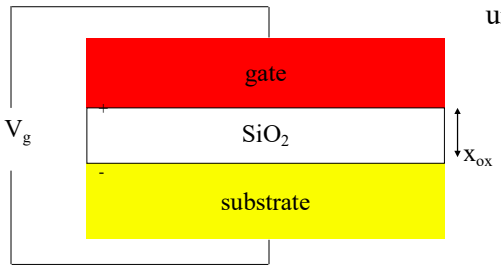


MOSFET as capacitor

- Basic structure of gate is parallel-plate capacitor:

Formula for parallel plate capacitance per unit area:

$C_{ox} = \varepsilon_{ox} / x_{ox}$



Threshold voltage

Components of threshold voltage V_t:

$$V_{t0} = V_{fb} + \phi_s + \frac{Q_b}{C_{ox}} + V_{II}$$

- V_{fb} = flatband voltage; depends on difference in work function between gate and substrate and on fixed surface charge. $V_{fb} = \Phi_{gs} - (Q_f / C_{ox})$
- ϕ_s = surface potential (about $2\phi_f$).
- $\frac{Q_b}{C_{ox}}$ Voltage on parallel plate capacitor.

$V_{II} = qD_I / C_{ox}$ Additional ion implantation.

Body effect

- Reorganize threshold voltage equation:

  $V_t = V_{t0} + \Delta V_t$
- Threshold voltage is a function of source/substrate voltage V_{sb}.
- Body effect γ is the coefficienct for the V_{sb} dependence factor.

Channel length modulation length parameter

- λ describes small dependence of drain current on V_{ds} in saturation.
- Factor is measured empirically.
- New drain current equation:
  - $I_d = 0.5k' (W/L)(V_{gs} - V_t)^2(1 - \lambda V_{ds})$
- Equation has a discontinuity between linear and saturation regions---small enough to be ignored.

Leakage and subthreshold current

- A variety of leakage currents draw current away from the main logic path.
- The subthreshold current is one particularly important type of leakage current.

Types of leakage current

- Weak inversion current (a.k.a. subthreshold current).
- Reverse-biased pn junctions.
- Drain-induced barrier lowering.
- Gate-induced drain leakage;
- Punchthrough currents.
- Gate oxide tunneling.
- Hot carriers.