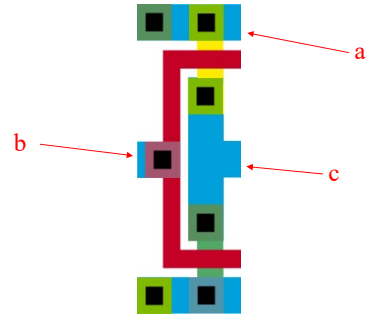
Paracitics
&
Delay Calculation

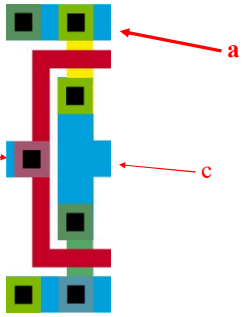
Parasitics and Performance

- Consider the following layout:
- What is the impact on performance of parasitics
  - At point a (VDD rail)?
  - At point b (input)?
  - At Point c (output)?



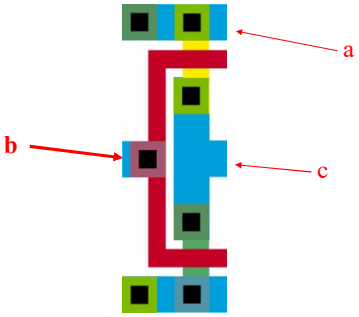
Parasitics and Performance

- a - power supply connections
  - capacitance - no effect on delay
  - resistance - increases delay (see p. 135)
    - minimize by reducing difffusion length
    - minimize using parallel vias



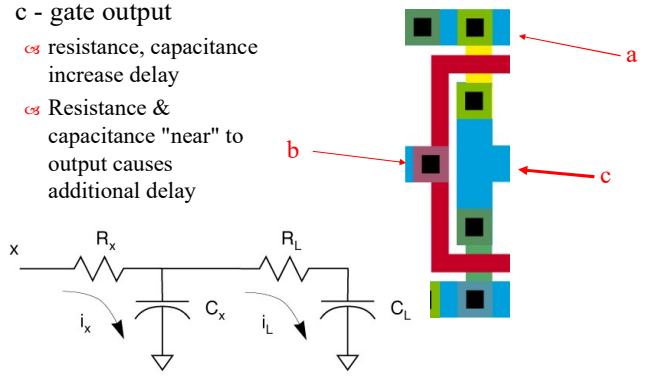
Parasitics and Performance

- b - gate input
  - capacitance increases delay on previous stage (often transistor gates dominate)
  - resistance increases delay on previous stage



Parasitics and Performance

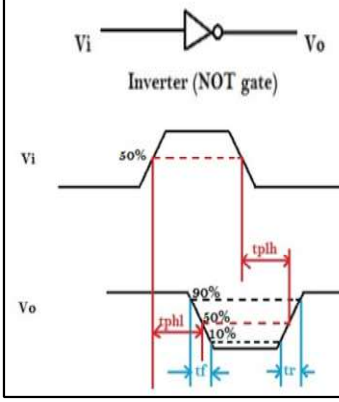
- c - gate output
  - resistance, capacitance increase delay
  - Resistance & capacitance "near" to output causes additional delay



Delay

Delay in VLSI refers to the **time** taken for a signal to propagate through a circuit. They describe various types of delays, including ***cell delay***, ***net delay***, and ***propagation delay***, as well as related concepts like rise time and fall time.

Ways of measuring gate delay

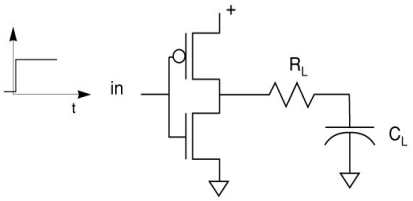


- Delay: time required for gate's output to reach 50% of final value.
- Transition time: time required for gate's output to reach 10% (logic 0) or 90% (logic 1) of final value.

tr = Rise transition time
tf = Fall transition time
tphl = Propagation delay high-low
tplh = Propagation delay low-high

Inverter Delay

It is necessary to take the load into account in even the simplest inverter delay analysis. ***The load on the inverter is a single resistor-capacitor (RC) circuit; the resistance and capacitance come from the logic gate connected to the inverter's output and the wire connecting the two.***



Delay assumptions

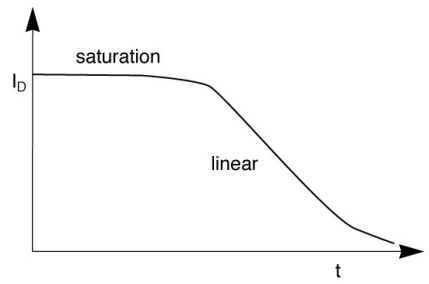
- Assume that only one transistor is on at a time. This gives two cases:
  - rise time, pullup on;
  - fall time, pullup off.
- Assume resistor model for transistor. Ignores saturation region and mischaracterizes linear region, but results are acceptable.

Delay Model

- λ model : Mead & Conway
- Current source model
- Fitted Model

Current through transistor

- Transistor starts in saturation region, then moves to linear region.



Capacitive Load

- **Unit load capacitance** C_l as 1/2 of the load capacitance of a minimum-size inverter driving another minimum-size inverter.
- C_l includes all the capacitances of the load transistors as well as the capacitances of the driving transistors that affect that node. In 80nm process ***Cl = 0.89 fF.***

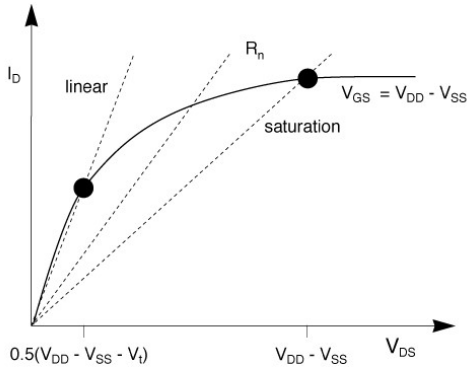
load capacitance $\boldsymbol{C_L}$ presented by another gate with different function and transistor sizes, we scale each transistor in the gate appropriately based on the transistor sizes

$$C_L = \sum_{1 \le i \le n} \frac{W}{L}_i C_l$$

Resistive model for transistor

- Average V/I at two voltages:
  - maximum output voltage
  - middle of linear region
- Voltage is V_{ds}, current is given I_d at that drain voltage. Step input means that $V_{gs} = V_{DD}$ always.

Resistive approximation



Transistor's Effective Resistance

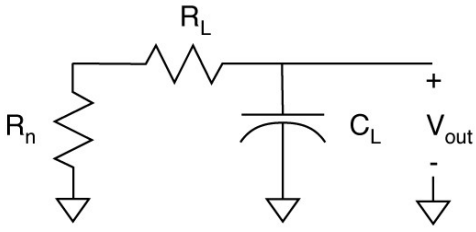
The table shows the effective resistance values for **minimum-size n-type and p-type** transistors in **180 nm** process The effective resistance of a transistor is scaled by ***L/W***:

type	V_{DD}-V_{SS} = 1.2V
R_n	**6.47 kΩ**
R_p	**29.6 kΩ**

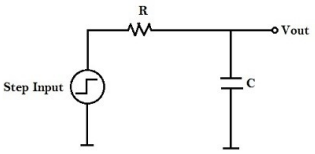
$$R_t = \frac{W}{L} R_{n,p}.$$

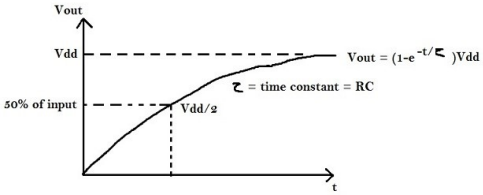
Inverter delay circuit

- Load is resistor + capacitor, driver is resistor.



Delay of a Minimum-Size Inverter





Propagation delay = 50% of input to 50% of output

R = Average 'ON' resistance of transistor
C = Output Capacitance

To find 't' at $V_{dd}/2$.
$V_{out} = (1-e^{-t/\tau})V_{dd}$,
$\tau = RC$= time constant.
Substituting 'V_{out}' equal to $V_{dd}/2$, and 't' equal to 't_p'
$V_{dd}/2 = (1-e^{-tp/\tau})\ V_{dd}$
$t_p = ln(2)\ \tau = 0.69\tau$

Inverter delay with τ model

- τ model: gate delay based on RC time constant τ.
- $V_{out}(t) = V_{DD} \exp\{-t/(R_n+R_L)/ C_{L}\}$
- $t_f = 2.2\ R\ C_L$
- For pullup time, use pullup resistance.