Wafer Preparation & Fabrication

Wafer Preparation…….

- End cropping
- Diameter grinding
- Crystal orientation, conductivity, and resistivity checking
- Grinding orientation indicators
- Wafer slicing
- Wafer marking
- Rough polishing
- Chemical mechanical polishing
- Backside processing
- Double-side polishing
- Wafer evaluation
- Oxidation
- Packaging

End cropping

After removal from the crystal grower, the crystal goes through a series of steps that result in the finished wafer. First is the cropping off of the crystal ends with a saw.

Diameter grinding

During crystal growth, there is a diameter variation over the length of the crystal. Diameter grinding is a mechanical operation performed in a in a centerless grinder. This machine grinds the crystal to the correct diameter without the necessity of clamping it into a lathe-type grinder with a fixed center point—although lathe-type grinders are used.

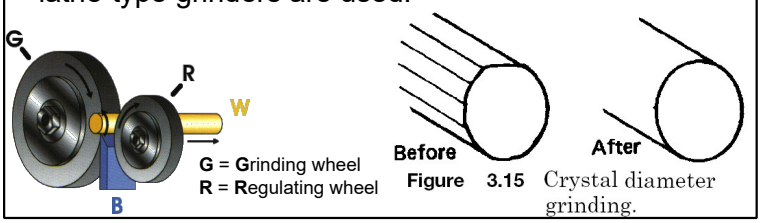


Figure 3.15 Crystal diameter grinding.

Crystal orientation, conductivity, and resistivity check

The crystal orientation (Fig. 3.16) is determined by either X-ray diffraction or collimated light refraction. X-rays or collimated light reflected off the crystal surface falls onto a photographic plate (Xrays) or screen (collimated light). The pattern formed on the plate or screen is indicative of the crystal plane .

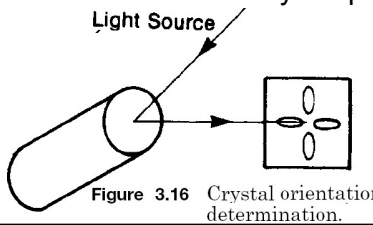


Figure 3.16 Crystal orientation determination.

Grinding orientation indicators

A ***flat***, called the major ***flat***, is ground along the axis. The ***flat*** functions as a visual reference to the orientation of the wafer.

A second, smaller, secondary ***flat*** is ground on the edge. The position of the secondary ***flat*** to the major ***flat*** tells the orientation and conductivity type of the wafer.

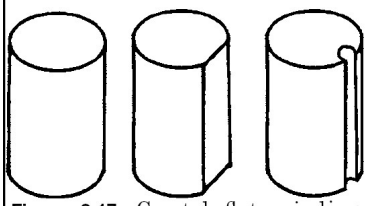


Figure 3.17 Crystal flat grinding.

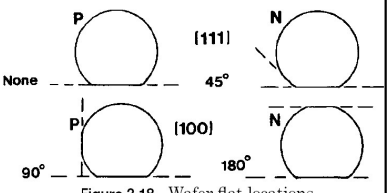
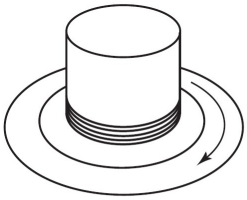


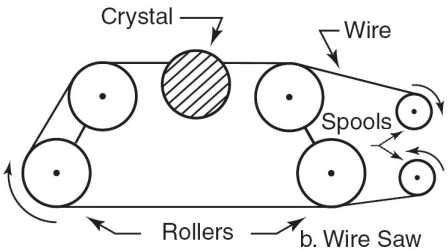
Figure 3.18 Wafer flat locations.

Wafer Slicing

The wafers are sliced from the crystal with the use of diamond-coated inside diameter saws (Fig. 3.19). For 300-mm diameter wafers, wire saws are used to ensure flat surfaces



a. Inside Diameter Diamond Saw



b. Wire Saw

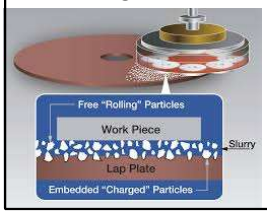
Wafer polishing

Rough Polish

Rough polishing is a conventional abrasive slurry lapping process to remove the surface damage left over from the wafer.

Chemical Mechanical Polishing (CMP)

The final polishing step is a combination of chemical etching and mechanical buffing.



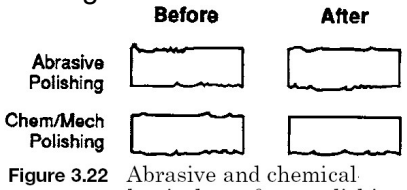


Figure 3.22 Abrasive and chemical-mechanical surface polishing.

Wafer Fabrication

Text book: Microchip Fabrication: A Practical Guide to Semiconductor Processing
By
Peter Van Zant
Capter-4: Wafer Preparation

Wafer Fabrication

Wafer fabrication is the manufacturing processes used to create the semiconductor devices in and on the wafer surface.

Wafer Terminology

1. Chip, die, device, circuit, microchip, or bar.
2. Scribe lines, saw lines, streets, & avenues.
3. Engineering die, test die.
4. Edge chips.
5. Wafer crystal planes.
6. Wafer flats/notches.

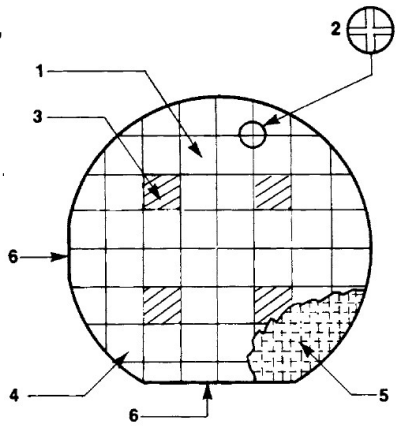


Figure 4.2 Wafer terminology.

Basic Wafer-Fabrication Operations

There are hundreds of thousands of different microchip types and functions. However, they are made with a small number of basic structures (primarily bipolar or MOS structures) and manufacturing processes.

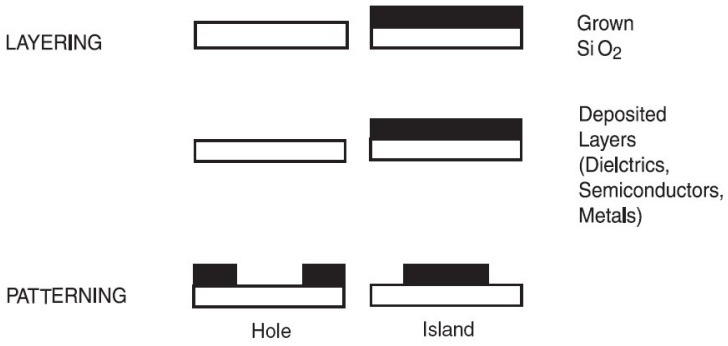
Basic steps of IC Fabrication

Followings are the basic steps used in an infinite number of sequences and variations to produce specific microchips.

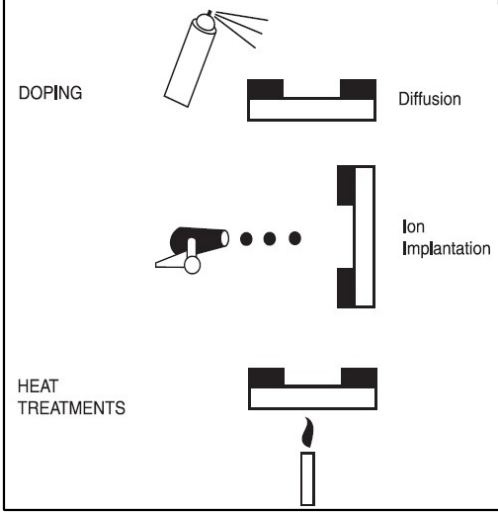
- ***Layering,***
- ***Patterning,***
- ***Doping, and***
- ***Heat treatment***

Basic IC Fabrication Operations

Layering, Patterning, Doping & Heat treatment are the basic steps used in an infinite number of sequences and variations to produce specific microchips.



Basic IC Fabrication operations…



1-Layering

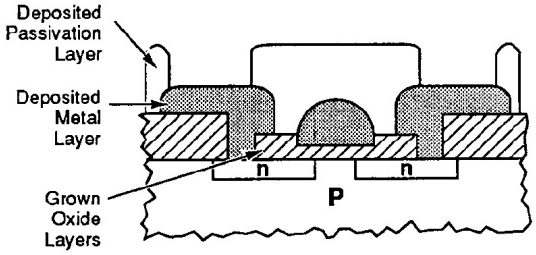


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Layering

- ***Grown*** (*Oxidation, Nitridation*)
- ***Deposited*** (*CVD, Sputtering, Evaporation, Electroplating*)

2-Patterning

- The patterning process is known by the names photomasking, masking, photolithography, and microlithography.
- Patterning is the series of steps that results in the removal of selected portions of the added surface layers

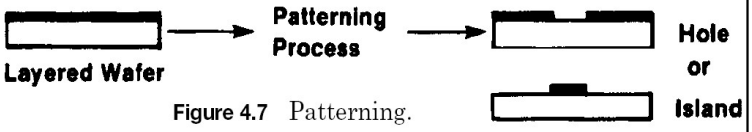


Figure 4.7 Patterning.

3-Doping

- Doping is the process that puts specific amounts of electrically active dopants in the wafer surface through openings in the surface layers
  - *thermal diffusion* and
  - *ion implantation*

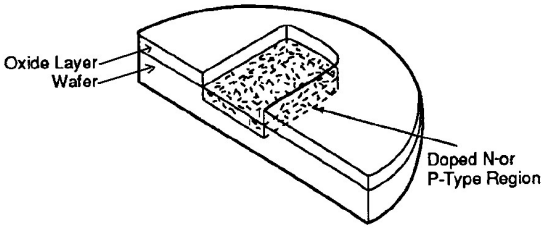


Figure 4.9 Formation of N- or P-type region in wafer surface.

4-Heat treatment

- Heat treatments are the operations in which the wafer is simply heated and cooled to achieve specific results

Operation	Heat treatment
Patterning	Soft bake Hard bake Post exposure bake (develop)
Doping	Post ion implant anneal
Layering	Post metal deposition and patterning anneal

Figure 4.10 Table of major heat treatments

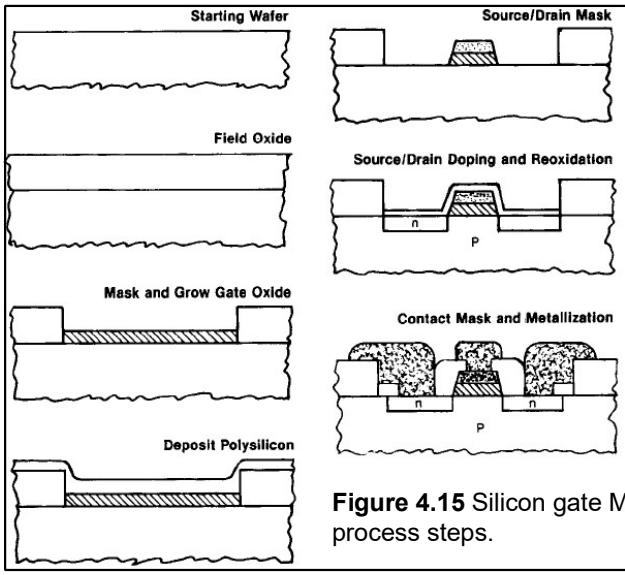


Figure 4.15 Silicon gate MOS process steps.

Step 1: Layering Operation. The building starts with an oxidation of the wafer surface to form a thin protective layer and to serve as a doping barrier. This silicon dioxide layer is called the *field oxide*.

Step 2: Patterning Operation. The patterning process leaves a hole in the field oxide that defines the location of the source, gate, and drain areas of the transistor.

Step 3: Layering Operation. Next, the wafer goes to an silicon dioxide oxidation operation. A thin oxide is grown on the exposed silicon. It will service as the gate oxide.

Step 4: Layering Operation. In step 4, another layering operation is used to deposit a layer of polycrystalline (poly) silicon. This layer will also become part of the gate structure.

Step 5: Patterning Operation. Two openings are patterned in the oxide/polysilicon layer to define the source and drain areas of the transistor.

Step 6: Doping Operation. A doping operation is used to create an N-type pocket in the source and drain areas.

Step 7: Layering Operation. Another oxidation/layering process is used to grow a layer of silicon dioxide over the source/drain areas.

Step 8: Patterning Operation. Holes, called contact holes, are patterned in the source, gate, and drain areas.

Step 9: Layering Operation. A thin layer of conducting metal, usually an aluminum alloy, is deposited over the entire wafer.

Step 10: Patterning Operation. After deposition, the wafer goes back to the patterning area where portions of the metallization layer are removed from the chip area and the scribe lines. The remaining portions connect all the parts of the surface components to each other in the exact pattern required by the circuit design.

Step 11: Heat Treatment Operation. Following the metal patterning step, the wafer goes through a heating process in a nitrogen gas atmosphere. The purpose of the step is to "alloy" the metal to the exposed source and drain regions and the gate region to ensure good electrical contact.

Step 12: Layering Operation. The final layer of this device is a protective layer known variously as a *scratch* or *passivation layer*. Its purpose is to protect the components on the chip surface during the testing and packaging processes, and during use.

Step 13: Patterning Operation. The last step in the sequence is a patterning process that removes portions of the scratch protection layer over the metallization terminal pads on the periphery of the chip. This step is known as the *pad mask*.