# Doping & Ion Implantation

**Cahpter-11 of Text**

## Doping

Doping is a process where a specific elements is introduced into intrinsic semiconductor materials to increase its conductivity. The doped material displays two unique properties that are the basis of solid-state electronics. The two properties are

1. Precise resistivity control through doping
2. Electron (***N-type***) and hole (***p-type***) conduction

## Junction

- A ***junction*** is the separation between a region that is rich in negative electrons (N-type region) and a region that is rich in holes (P-type region). The exact location of a junction is where the concentration of electrons equals the concentration of holes. The usual way to form junctions in the surface of semiconductor wafer is by
  - » ***thermal diffusion***
  - » ***ion implantation***

## Diffusion

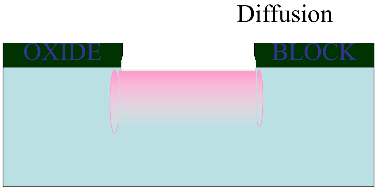
Two conditions are necessary for a diffusion to take place

- – higher concentration
- – sufficient energy

The goals of solid-state:

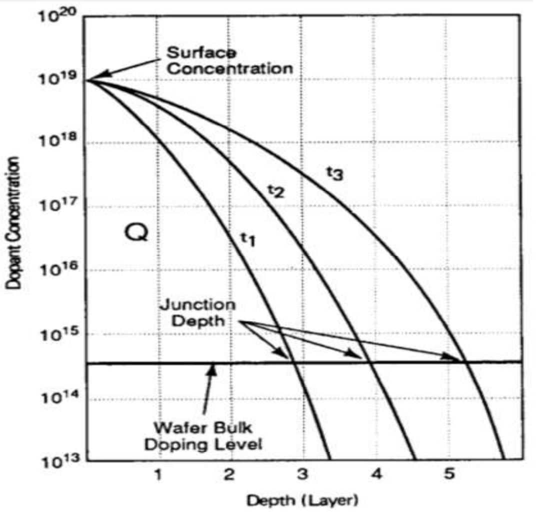
1. The creation of a specific number (concentration) of dopant atoms in the wafer surface
2. To create an N-P (or P-N) junction at a specific distance below the wafer surface
3. To create a specific distribution and concentration of dopant atoms in the wafer surface

# Diffusion: Steps



1. Pre Clean
   - To remove particles
   - Thin oxide grows
2. HF Etch
   - To remove oxide
   - Not too much!
3. Deposit (pre dep)
   - Deposit enough to be higher than the solubility limit
4. Drive In
   - High temp to enable diffusion inside Si
   - Also forms $SiO_2$ (with high dopant concentration)
   - 2-STEP diffusion (usual)
5. Deglaze (HF Etch)
   - Oxide may act as dopant source in future steps
   - Removing highly doped oxide may be problem (for dry etch)

# Dopant Profile



Typical dopant profile for 3 different deposition times.

# Diffusion mechanism

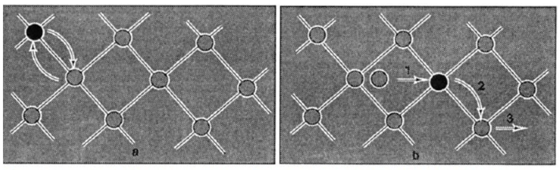


Figure 11.12 Diffusion models. (a) Vacancy & (b) interstitial model

# Doped Region by Diffusion

After patterning a hole in the oxide layer, the wafer is exposed to dopant at high temp in a diffusion tube.

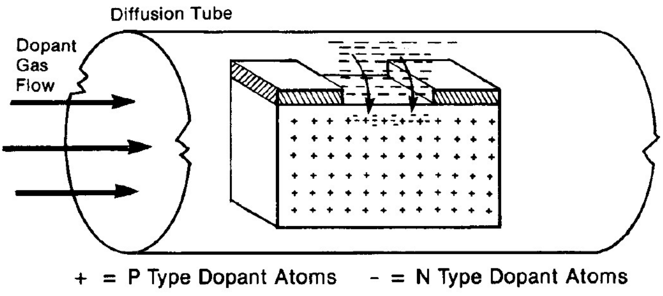


**Figure 11.4** Start of a diffusion process.

# Dopant amounts and level conductivity type

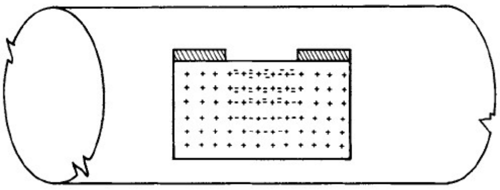
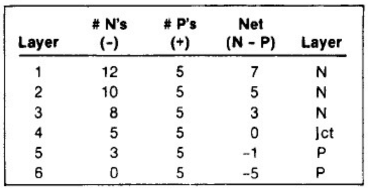


Figure 11.5 Cross section of wafer at conclusion of diffusion.



| Layer | # N's (-) | # P's (+) | Net (N - P) | Layer |
|---|---|---|---|---|
| 1 | 12 | 5 | 7 | N |
| 2 | 10 | 5 | 5 | N |
| 3 | 8 | 5 | 3 | N |
| 4 | 5 | 5 | 0 | Jct |
| 5 | 3 | 5 | -1 | P |
| 6 | 0 | 5 | -5 | P |

Figure 11.6 Dopant amounts and level conductivity type.

# Diffusion Process Steps

The use of solid-state *thermal diffusion* to create junctions in semiconductor wafers requires two steps.

- *deposition,* and
- *drive-in oxidation*.

# Deposition

The first step of a diffusion process is called *deposition*; it is also called ***predeposition***, ***dep***, or ***predep***.

A deposition process is controlled or limited by ***two*** factors

- ***Diffusivity,*** the rate (speed) of movement of the dopant through the particular wafer material
- ***maximum solid solubility,*** the max. concentration of a specific dopant that can be put into the wafer

# Deposition steps

A deposition process requires four steps.

1. Preclean and etch
2. Tube deposition
3. Deglaze
4. Evaluation

# Deposition process

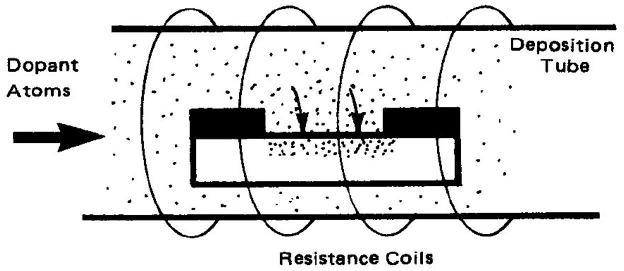


**Figure 11.11** Deposition.

# Preclean and etch

- In *preclean* step
  - – mechanical scrubbering,
  - – RCA wet cleaning sequence to remove organic and inorganic contamination.
    - step-1: (*organic residues cleaning*) uses a solution of water, hydrogen peroxide, and ammonium hydroxide.
    - step-2: (*alkali ions and hydroxides and complex residual metals cleaning*) solution of water, $H_2O_2$, and HCl mixed in ratios of 6:1:1 to 8:2:1 and is used at the 75°C to 85°C range.
  - – Finally, an HF or diluted HF etch is performed to rid the surface of native or chemically grown oxides.
- In *etch* step
  - – the wafers is chemically etched in an HF or HF and water solution to remove any native oxide that may have grown on the exposed silicon surface.

# Deposition

Deposition requires a minimum of ***three cycles***.

- – ***loading*** cycle, which takes place in a nitrogen atmosphere.
- – ***doping*** cycle.
- – ***exit*** cycle, which also takes place in a nitrogen atmosphere

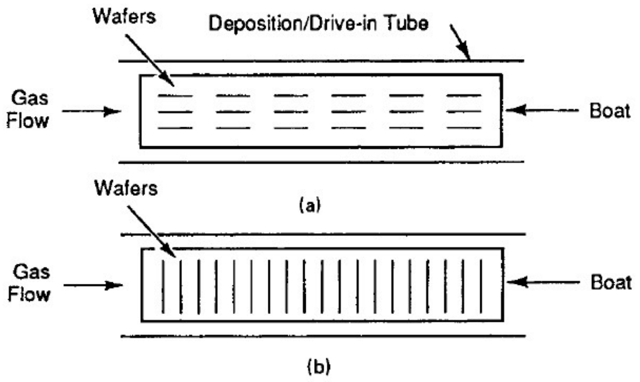


**Figure 11.15** Boat loading (*a*) Parallel and (*b*) perpendicular.

# Perpendicular Vs Parallel placement of wafers in diffusion tube

- Perpendicular (right-angle to the tube axis) placement is the highest packing density, but it can cause uniformity problems, because the wafers act as baffles to the gas flow.
- Parallel placement offers the advantage of more uniform doping, since the doping gas proceeds unimpeded through the wafer boat.

# Deglaze

During the deposition cycle, the formed native oxide gets doped and later can act as an unwanted source of dopant during the drive-in-oxidation step.

- *Deposition created oxide can be difficult to etch, causing incomplete etch in a subsequent masking process.*

The term ***deglaze*** is used to cover the removal of any silicon oxide, diffusion (phosphorus and boron) glass, or nitride coating

- The oxide is removed from the surface by immersion in a diluted HF solution, followed by a water rinse and a drying step.

# Evaluation

- Sheet resistance
- C-V measurement to see the surface contaminations
- UV light to see the dirt

# Drive-in Oxidation

Also known as ***drive-in***, ***diffusion***, ***reoxidation***, and ***reox.*** The purpose of this step is :

- redistribution of the dopant and
- growth of a new oxide layer

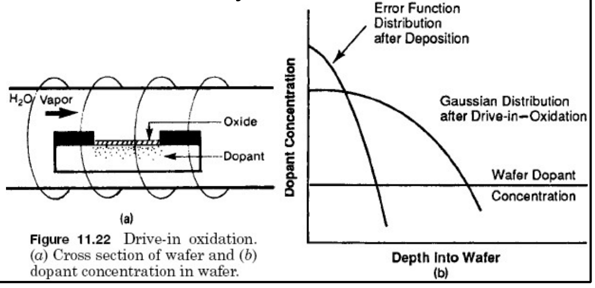


**Figure 11.22** Drive-in oxidation. (*a*) Cross section of wafer and (*b*) dopant concentration in wafer.

# Ion Implantation

Thermal diffusion places a limit on the production of advanced circuits because of

- lateral diffusion,
- ultra thin junctions,
- poor doping control,
- surface contamination interference, and
- dislocation generation.

***Ion implantation*** overcomes these limits of diffusion and also adds additional benefits.

# Ion Implantation

- No side diffusion,
- ~ room temperature process,
- Dopant goes inside the silicon
- Controlled doping
  - concentration
  - profile (depth)

# Concept of Ion Implantation

- Ion implantation is a physical process while Diffusion is a chemical process. The dopant atoms physically bombard the wafer, enter the surface, and come to rest below the surface

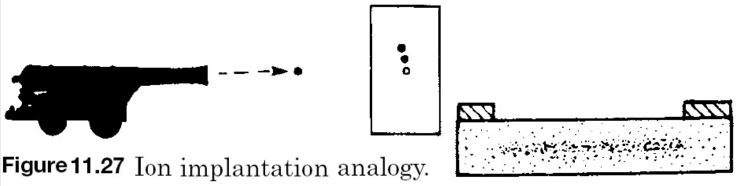
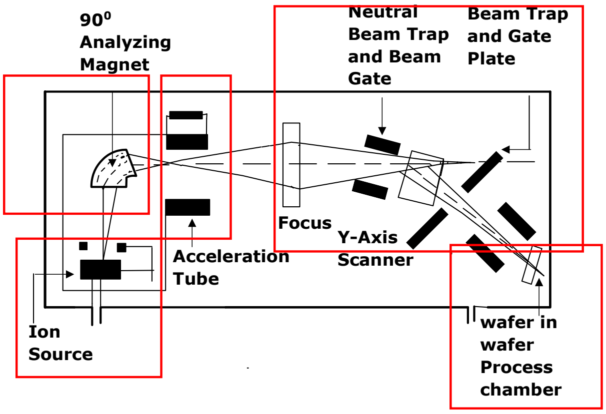


**Figure 11.27** Ion implantation analogy.

# Ion Implantation System



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# 1. Ion Source

- Gas or solid source (no liquid source)
- Solid heated to obtain vapor ($P_2O_5$)
  - effectively gas source

$AsF_5, BF_3, SbF_3, PF_3, PF_5$

- Ionization chamber
  - low pressure (milli/ micro torr) to ionize
  - heated filament (thermionic emission)
  - positively charged ions created

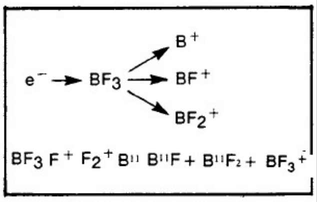
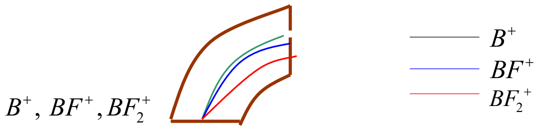


**Figure 11.29** Ion species of $BF_3$.

# 2. Analyzing

- Selection, analyzing, mass analyzing, ion separation
- Magnetic field to control the path
- Charge to Mass Ratio
- Some of the species from $BF_3$ source
- Selection of $B^+$



# 3. Acceleration

- Acceleration needed for implantation
- Positive ions accelerated with ring anodes
- Energy range: 5 keV for low, 2 MeV for high
- Beam Focus (magnetic/electric)

# 4. Scanning

Electrical (beam) scanning & Mechanical (wafer) scanning

- Beam Scan:

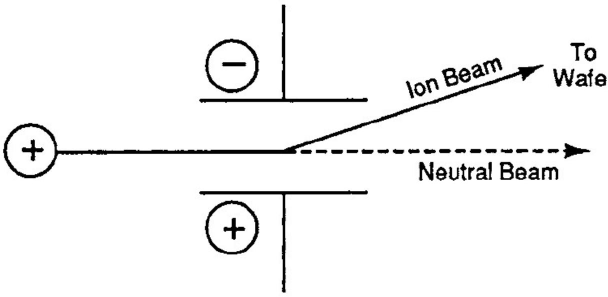


**Figure 11.32** Deflection of ion beam