Delay

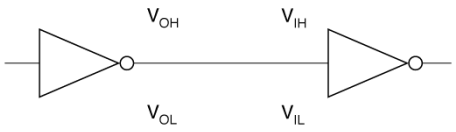
- Logic level
- Transistor resistance calculation
- Delay calculation

Logic levels

- Solid logic 0/1 defined by V_{SS}/V_{DD}.
- Inner bounds of logic values V_L/V_H are not directly determined by circuit properties, as in some other logic families.

Logic level matching

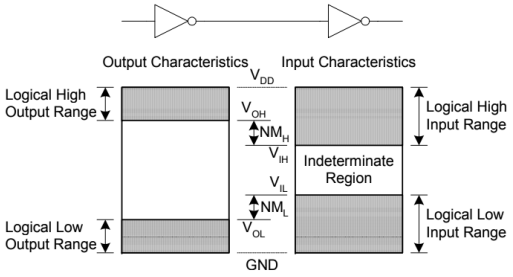
- Levels at output of one gate must be sufficient to drive next gate.



If the gates are to work together, we must ensure that $V_{OL}<V_{IL}$ *and* $V_{OH}> V_{IH}$.

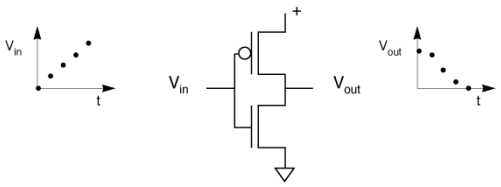
Noise Margins

How much noise can a gate input see before it does not recognize the input?



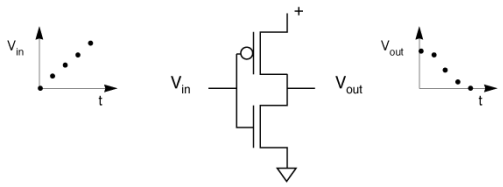
Transfer characteristics

- Transfer curve shows static input/output relationship—hold input voltage, measure output voltage.



Transfer characteristics

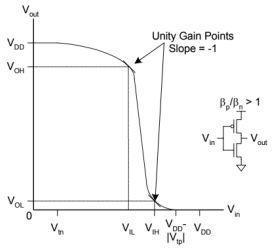
- Transfer curve shows static input/output relationship—hold input voltage, measure output voltage.



Inverter transfer curve

To maximize noise margins, select logic levels at

– unity gain point of DC transfer characteristic



Logic thresholds

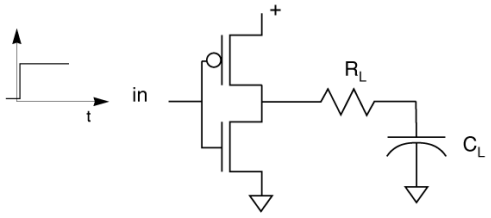
- Choose threshold voltages at points where slope of transfer curve = -1.
- Inverter has a high gain between V_{IL} and V_{IH} points, low gain at outer regions of transfer curve.
- Note that logic 0 and 1 regions are not equal sized—in this case, high pullup resistance leads to smaller logic 1 range.

Noise margin

- Noise margin = voltage difference between output of one gate and input of next. Noise must exceed noise margin to make second gate produce wrong output.

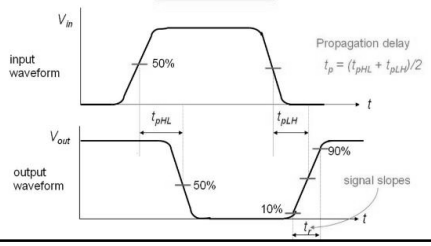
Delay

- Assume ideal input (step), RC load.



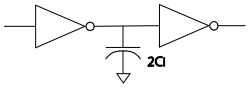
Delay assumptions

- Assume that only one transistor is on at a time. This gives two cases:
  - rise time, pullup on;
  - fall time, pullup off.



Capacitive load

- Most capacitance comes from the next gate.
- Load is measured or analyzed by Spice.
- C_l: load presented by one minimum-size transistor.

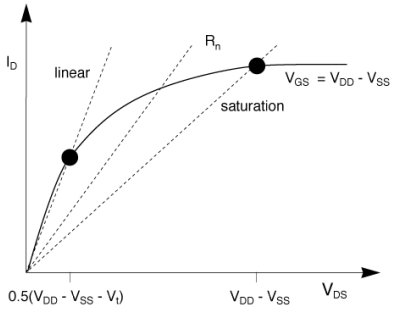


$C_L = \Sigma (W/L)_i C_l$

Resistive model for transistor

- Average V/I at two voltages:
  - maximum output voltage
  - middle of linear region
- Voltage is V_{ds}, current is given I_d at that drain voltage. Step input means that $V_{gs} = V_{DD}$ always.

Resistive approximation



A more accurate approach is to assume the resistance from the *fit* of the delay data obtained from Spice simulation. In 180 nm technology

type	V_{DD}-V_{SS} = 1.2V
R_n	**6.47 kΩ**
R_p	**29.6 kΩ**

Effective resistance

$$R_t = \frac{W}{L} R_{n,p}$$

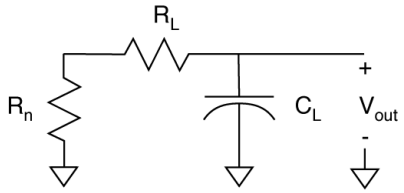
Simple models become less in nanometer technologies.

Ways of measuring gate delay

- Delay: time required for gate's output to reach 50% of final value.
- Transition time: time required for gate's output to reach 10% (logic 0) or 90% (logic 1) of final value.

Inverter delay circuit

- Load is resistor + capacitor, driver is resistor.



Inverter delay with τ model

- τ model: gate delay based on RC time constant τ.
- $V_{out}(t) = V_{DD} \exp\{-t/[(R_n+R_L)C_L]\}$
- $t_f = 2.2\ R\ C_L$
- For pullup time, use pullup resistance.

τ model inverter delay

- 0.180 nm process:
  - $R_n = 6.47\ k\Omega$
  - $C_l = 0.89$ fF
  - $C_L = 1.78$ fF
- So
  - $t_d = 0.69 \times 6.47E3 \times 1.78E\text{-}15 = 7.8$ ps.
  - $t_f = 2.2 \times 6.47E3 \times 1.78E\text{-}15 = 26.4$ ps.