Power consumption analysis

- Almost all power consumption comes from switching behavior.
- Static power dissipation comes from leakage currents.
- Surprising result: power consumption is independent of the sizes of the pullups and pulldowns.

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Power consumption circuit

■ Input is square wave.

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Power consumption

- A single cycle requires one charge and one discharge of capacitor: $E = C_L(V_{DD} V_{SS})^2$.
- Clock frequency f = 1/t.
- Energy $E = C_L(V_{DD} V_{SS})^2$.
- Power = E x f = f $C_L(V_{DD} V_{SS})^2$.

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Observations on power consumption

- Resistance of pullup/pulldown drops out of energy calculation.
- Power consumption depends on operating frequency.
 - Slower-running circuits use less power (but not less energy to perform the same computation).

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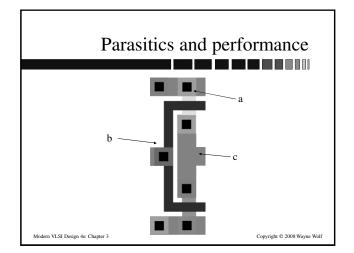
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Speed-power product

- Also known as power-delay product.
- Helps measure quality of a logic family.
- For static CMOS:
 - $-SP = P/f = CV^2.$
- Static CMOS speed-power product is independent of operating frequency.
 - Voltage scaling depends on this fact.

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Effect of parasitics

 a: Capacitance on power supply is not bad, can be good in absence of inductance.
Resistance slows down static gates, may cause pseudo-nMOS circuits to fail.

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Effects of parasitics, cont'd

- b: Increasing capacitance/resistance reduces input slope.
- c: Similar to parasitics at b, but resistance near source is more damaging, since it must charge more capacitance.

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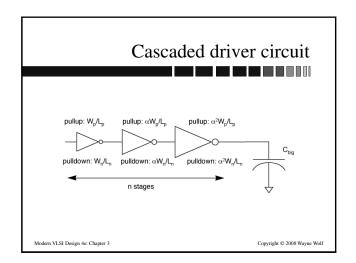
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Driving large loads

- Sometimes, large loads must be driven:
 - off-chip;
 - long wires on-chip.
- Sizing up the driver transistors only pushes back the problem—driver now presents larger capacitance to earlier stage.

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Optimal sizing

- Use a chain of inverters, each stage has transistors a larger than previous stage.
- Minimize total delay through driver chain:

$$-t_{tot} = n(C_{big}/C_g)^{1/n} t_{min}.$$

■ Optimal number of stages:

$$- n_{opt} = \ln(C_{big}/C_g).$$

■ Driver sizes are exponentially tapered with size ratio α .

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