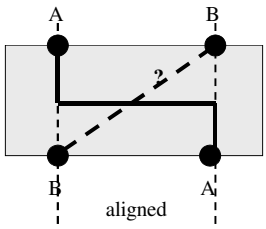
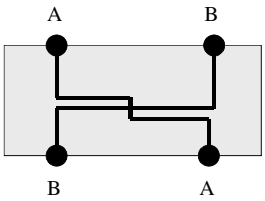
Limitations of left-edge algorithm

- Some combinations of nets require more than one horizontal segment per net.



Dogleg wire

- A dogleg wire has more than one horizontal segment.



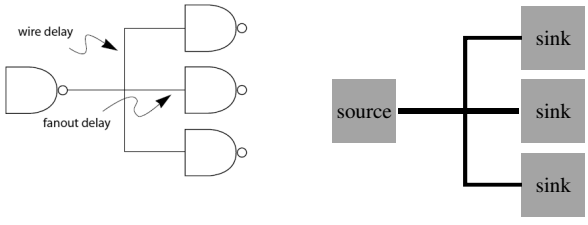
Combinational network delay.

Sources of delay

- Gate delay:
  - drive;
  - load.
- Wire:
  - lumped load;
  - transmission line.

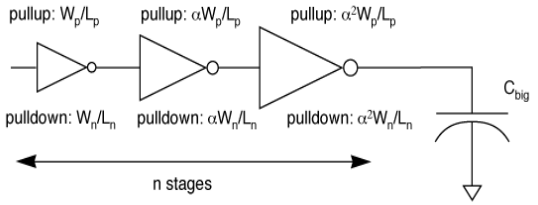
Fanout

- Fanout adds capacitance.



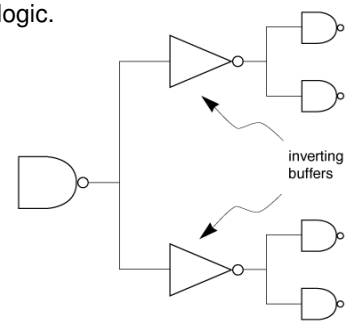
Ways to drive large fanout

- Increase sizes of driver transistors. Must take into account rules for driving large loads.



Buffers

Add intermediate buffers. This may require/allow restructuring of the logic.

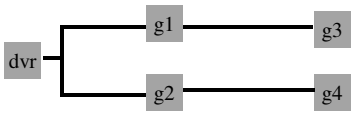


Wire capacitance

- Use layers with lower capacitance.
- Redesign layout to reduce length of wires with excessive delay.

Placement and wire capacitance

unbalanced load



more balanced