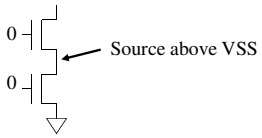
# Power Consumption in gates




# Body effect and gates

- Difference between source and substrate voltages causes body effect.
- Source for gates in middle of network may not equal substrate:

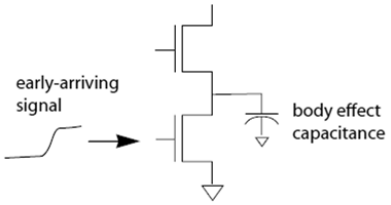






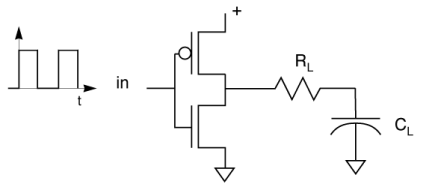
# Body effect and gate input ordering

- To minimize body effect, put early arriving signals at transistors closest to power supply:



## Power consumption circuit

- Input is square wave.







## Power consuming Sources

Power is consumed by gates in two different ways:

- **dynamic power** is consumed when gates drive their outputs to new values;
- **static power** is consumed even when the gate is quiet and its output is not changing.

We can summarize this observation in a formula:

$$P=P_D + P_S$$




## Power consumption analysis

- Almost all power consumption comes from switching behavior.
- Static power dissipation comes from leakage currents.
- Surprising result: power consumption is independent of the sizes of the pullups and pulldowns.

## Power consumption

$$i_{CL}(t) = \frac{V_{DD}-V_{SS}}{R_p} e^{-(t/R_pC_L)}, \qquad v_{CL}(t) = (V_{DD}-V_{SS})[1-e^{-(t/R_pC_L)}].$$

$$E_C = \int_0^\infty i_{C_L}(t) v_{C_L}(t)) dt = C_L(V_{DD}-V_{SS})^2 \left(e^{-t/R_pC_L} - \frac{1}{2} e^{-2t/R_pC_L}\right)\Big|_0^\infty = \frac{1}{2} C_L(V_{DD}-V_{SS})^2$$

- A single cycle requires one charge and one discharge of capacitor: $E = C_L(V_{DD} - V_{SS})^2$ .
- Clock frequency f = 1/t.
- Energy $E = C_L(V_{DD} - V_{SS})^2$.
- Power = E x f = f $C_L(V_{DD} - V_{SS})^2$.




## Observations on power consumption

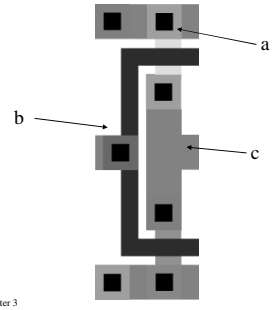
- Resistance of pullup/pulldown drops out of energy calculation.
- Power consumption depends on operating frequency.
  - Slower-running circuits use less power (but not less energy to perform the same computation).




## Speed-power product

- Also known as power-delay product.
- Helps measure quality of a logic family.
- For static CMOS:
  - $SP = P/f = CV^2$.
- Static CMOS speed-power product is independent of operating frequency.
  - Voltage scaling depends on this fact.

## Parasitics and performance

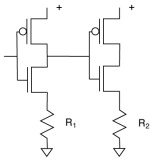






## Effect of parasitics

- a: Capacitance on power supply is not bad, can be good in absence of inductance. Resistance slows down static gates, may cause pseudo-nMOS circuits to fail.

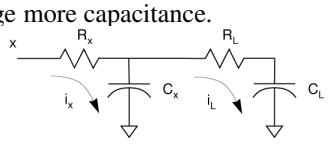






## Effects of parasitics, cont'd

- b: Increasing capacitance/resistance reduces input slope.
- c: Similar to parasitics at b, but resistance near source is more damaging, since it must charge more capacitance.

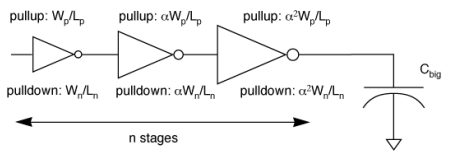


## Driving large loads

- Sometimes, large loads must be driven:
  - off-chip;
  - long wires on-chip.
- Sizing up the driver transistors only pushes back the problem—driver now presents larger capacitance to earlier stage.




## Cascaded driver circuit







## Optimal sizing

- Use a chain of inverters, each stage has transistors a larger than previous stage.
- Minimize total delay through driver chain:
  - $t_{tot} = n(C_{big}/C_g)^{1/n} t_{min}$.
- Optimal number of stages:
  - $n_{opt} = \ln(C_{big}/C_g)$.
- Driver sizes are exponentially tapered with size ratio $\alpha$.