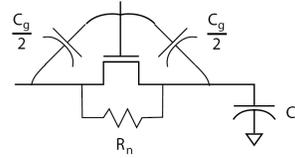


Topics

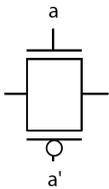
- n Switch Logic
- n Pseudo-nMOS gates.
- n DCVS logic.
- n Domino gates.

n-type Switch



- n It requires only one transistor and one gate signal. It transmits a logic 0 well, but when V_{DD} is applied to the drain, the voltage at the source is $(V_{DD} - V_{in})$.
- n When switch logic drives gate logic, n-type switches can cause electrical problems.

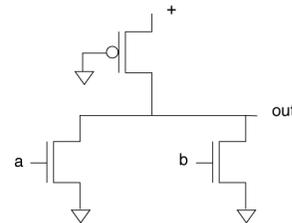
Transmission gate



- n when V_{DD} or V_{SS} is applied to the drain, V_{DD} or V_{SS} appears at the source.
- n It requires
 - two transistors and their associated tubs;
 - both true and complement forms of the gate signal

Pseudo-nMOS

- n Uses a p-type as a resistive pullup, n-type network for pulldowns.



Characteristics

- n Consumes static power.
- n Has much smaller pullup network than static gate.
- n Pulldown time is longer because pullup is fighting.

Output voltages

- n Logic 1 output is always at V_{DD} .
- n Logic 0 output is above V_{SS} .
- n $V_{OL} = 0.25 (V_{DD} - V_{SS})$ is one plausible choice.

Producing output voltages

- n For logic 0 output, pullup and pulldown form a voltage divider.
- n Must choose n, p transistor sizes to create effective resistances of the required ratio.
- n Effective resistance of pulldown network must be computed in worst case—series n-types means larger transistors.

Transistor ratio calculation

- n In steady state logic 0 output:
 - pullup is in linear region, $V_{ds} = V_{out} - (V_{DD} - V_{SS})$;
 - pulldown is in saturation.
- n Pullup and pulldown have same current flowing through them.

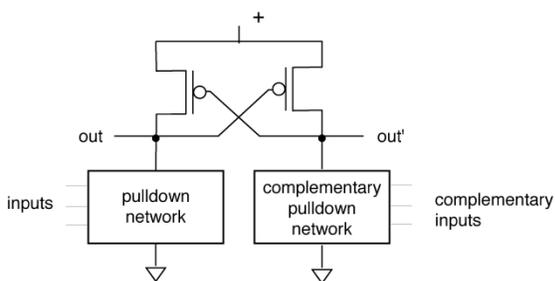
Transistor ratio, cont'd.

- n Equate two currents:
 - $I_{dp} = I_{dd}$.
- n Using 0.5 μm parameters, 3.3V power supply:
 - $W_p/L_p / W_n/L_n = 3.9$.

DCVS logic

- n DCVSL = differential cascode voltage logic.
- n Static logic—consumes no dynamic power.
- n Uses latch to compute output quickly.
- n Requires true/complement inputs, produces true/complement outputs.

DCVS structure



DCVS operation

- n Exactly one of true/complement pull-down networks will complete a path to the power supply.
- n Pull-down network will lower output voltage, turning on other p-type, which also turns off p-type for node which is going down.

DCVS example

