**Topics**

- Switch Logic
- Pseudo-nMOS gates.
- DCVS logic.
- Domino gates.

**n-type Switch**

- It requires only one transistor and one gate signal. It transmits a logic 0 well, but when $V_{DD}$ is applied to the drain, the voltage at the source is $(V_{DD} - V_{in})$.
- When switch logic drives gate logic, n-type switches can cause electrical problems.

**Transmission gate**

- when $V_{DD}$ or $V_{SS}$ is applied to the drain, $V_{DD}$ or $V_{SS}$ appears at the source.
- It requires
  - two transistors and their associated tubs;
  - both true and complement forms of the gate signal

**Pseudo-nMOS**

- Uses a p-type as a resistive pullup, n-type network for pulldowns.
Characteristics

- Consumes static power.
- Has much smaller pullup network than static gate.
- Pulldown time is longer because pullup is fighting.

Output voltages

- Logic 1 output is always at $V_{DD}$.
- Logic 0 output is above $V_{SS}$.
- $V_{OL} = 0.25 (V_{DD} - V_{SS})$ is one plausible choice.

Producing output voltages

- For logic 0 output, pullup and pulldown form a voltage divider.
- Must choose n, p transistor sizes to create effective resistances of the required ratio.
- Effective resistance of pulldown network must be computed in worst case—series n-types means larger transistors.

Transistor ratio calculation

- In steady state logic 0 output:
  - pullup is in linear region, $V_{ds} = V_{out} - (V_{DD} - V_{SS})$;
  - pulldown is in saturation.
- Pullup and pulldown have same current flowing through them.
Transistor ratio, cont’d.

- Equate two currents: \( I_{dp} = I_{dd} \).
- Using 0.5 mm parameters, 3.3V power supply:
  \( W_{p}/L_{p} / W_{n}/L_{n} = 3.9 \).

DCVS logic

- DCVSL = differential cascode voltage logic.
- Static logic—consumes no dynamic power.
- Uses latch to compute output quickly.
- Requires true/complement inputs, produces true/complement outputs.

DCVS structure

DCVS operation

- Exactly one of true/complement pulldown networks will complete a path to the power supply.
- Pulldown network will lower output voltage, turning on other p-type, which also turns off p-type for node which is going down.
The simplest way to reduce the operating voltage of a gate is to connect it to a lower power supply. We saw the relationship between power supply voltage and power consumption in Section 3.3.5:

- For large $V_t$, Equation 3.7 tells us that delay changes linearly with power supply voltage.
- Equation 3.15 tells us that power consumption varies quadratically with power supply voltage.

### Delay in Wires: Lumped RC Model

Lumped RC Model:

- Delay time constant (ignoring driving gate)
  \[ \tau = R \times C = (r \times L / W) \times (L \times w \times C_{\text{plate}}) \]
  \[ = r \times c \times L^2 \]

- Problem: Overly Pessimistic

### Delay in Long Wires - Distributed RC Model

- Alternative: Break wire into small segments

- Approx. Solution - 1st moment of impulse response
  \[ \tau = \frac{r \times c \times L}{2} \]

- Important: Delay still grows as square of length
Delay in Long Wires -
Consequences in design

- Distributed RC model:
  \[ \tau_{\text{delay}} = \frac{\text{RC}}{2} \]

- Delay grows as square of L!
  - Choose wire material that minimizes \( r, c \)
  - Break wire into buffered segments to optimize delay

Elmore Delay

- Consider R-C ladder network with unequal values

  \[ \tau_N = \sum_{i=1}^{N} \sum_{j=1}^{i} c_i r_j \]

  \[ \tau_i = c_i r_i (r_1 + r_2 + \ldots + r_i) \]

Elmore Delay Applications

- Wire sizing to minimize delay
- Delay prediction of complex networks
  (as long as they take the form of a ladder)

Wire Sizing

- Recall distributed model of wire: multiple segments

  \[ \tau_i = c_i r_i (r_1 + r_2 + \ldots + r_i) \]

  note strong impact of \( r_1 \), lesser impact of \( r_2 \), etc

  Idea: Reduce overall delay by tapering segments
  - Make Segment 1 widest to reduce \( r_1 \) (increases \( C_1 \))
  - Make Segment 2 less wide to reduce \( r_2 \) (increases \( C_2 \))
  - etc.
Wire Sizing

- Ideal Result wire should taper exponentially
  - see Eq. 3-20, p. 163 [Fis95]:

More pragmatic approach: step-tapered wire


Delay in RC-Trees

- Many interconnection networks are trees
  - Extracted RC circuit modeling a gate output
  - Clock trees

Delay in RC-Trees:
Penfield-Rubenstein Bounds

- Key idea: characterize time constants in terms of
  - Path resistances between nodes
    \[ R_{km} = \sum R_j \Rightarrow (R_j \in \{\text{path(in} \rightarrow \text{out}) \cap \text{path(k} \rightarrow \text{out})\) \]
  - Capacitance values at each node

Elmore Delay Problem

- What are the Elmore time constants \( \tau_1, \tau_2, \tau_3 \)?