Chapter-4: Combinational Logic Networks

Topics

The knowledge of logic gates, developed in the last chapter, will be used to analyze the delay and testability properties of combinational logic networks, including both the interconnect and the gates.

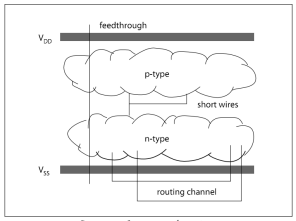
Placement & Routing

- Standard cell-based layout.
  - Small gates, MUXs, Flipflops etc.
- Channel routing.

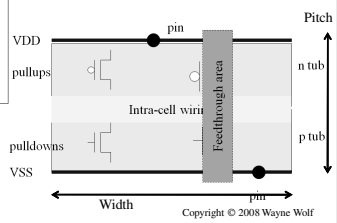
Standard cell layout

- Layout made of small cells: gates, flip-flops, etc.
- Cells are hand-designed.
- Placement & Routing

Standard cell structure



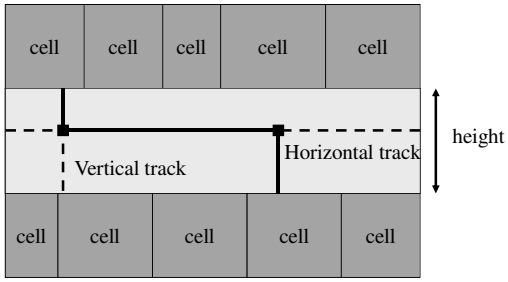
Structure of a one-row layout.



Standard cell design

- Pitch: height of cell.
  - All cells have same pitch, may have different widths.
- VDD, VSS connections are designed to run through cells.
- A feedthrough area may allow wires to be routed over the cell.

Placement of Cells



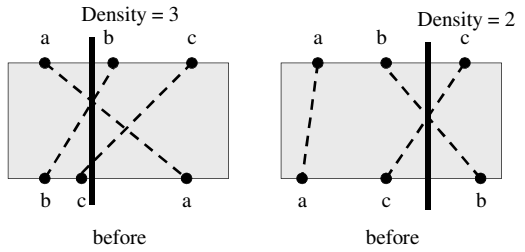
Routing channels

- Tracks form a grid for routing.
  - Spacing between tracks is center-to-center distance between wires.
  - Track spacing depends on wire layer used.
- Different layers are (generally) used for horizontal and vertical wires.
  - Horizontal and vertical can be routed relatively independently.

Routing channel design

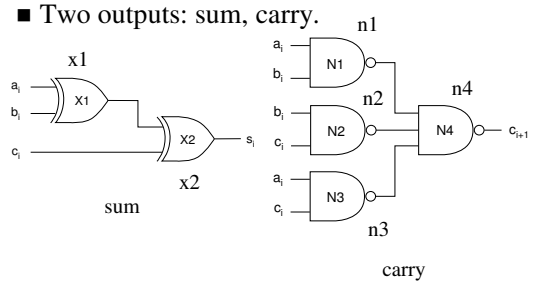
- Placement of cells determines placement of pins.
- Pin placement determines difficulty of routing problem.
- Density: lower bound on number of horizontal tracks needed to route the channel.
  - Maximum number of nets crossing from one end of channel to the other.

Pin placement and routing



Example: full adder layout

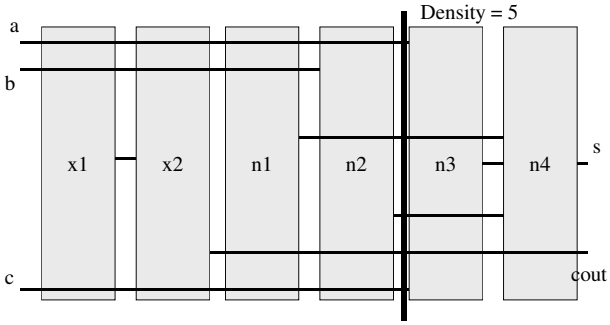
- Two outputs: sum, carry.



Layout methodology

- Generate candidates, evaluate area and speed.
  - Can improve candidate without starting from scratch.
- To generate a candidate:
  - place gates in a row;
  - draw wires between gates and primary inputs/outputs;
  - measure channel density.

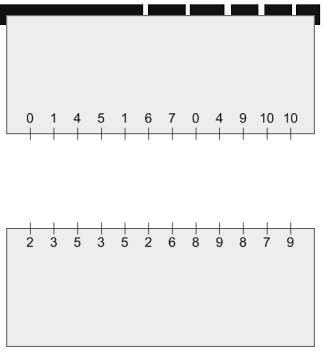
A candidate layout



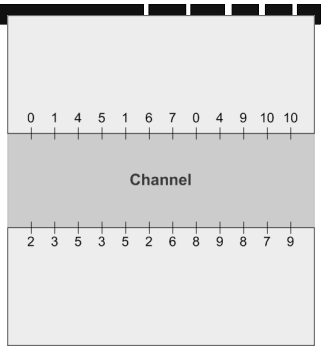
Improvement strategies

- Swap pairs of gates.
  - Doesn't help here.
- Exchange larger groups of cells.
  - Swapping order of sum and carry groups doesn't help either.
- This seems to be the placement that gives the lowest channel density.
  - Cell sizes are fixed, so channel height determines area.

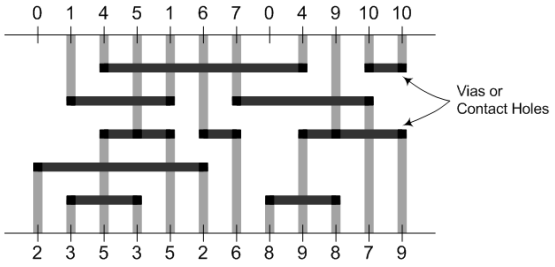
A Channel Routing Problem



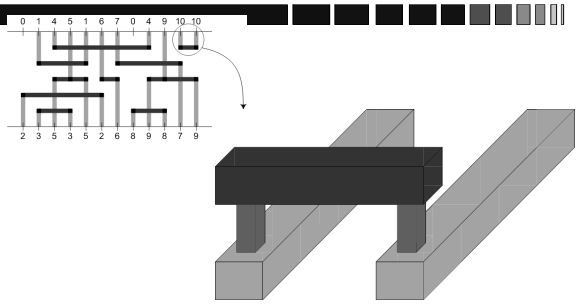
A Channel Routing Problem (cont'd)



A Solution to the Channel Routing Problem

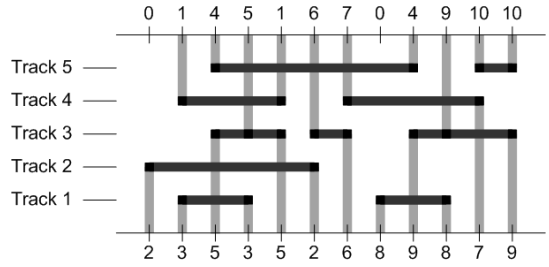


A Solution to the Channel Routing Problem (in VLSI Physical Design)



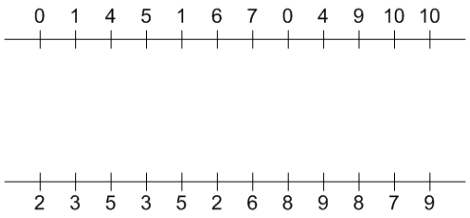
- Different colors represent different layers.

A Solution to the Channel Routing Problem (cont'd)



Minimizing the number of tracks means minimizing the routing area.

A Channel Routing Problem



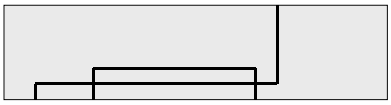
The Left-Edge Algorithm

- Proposed by Hashimoto and Stevens in 1971
- Regarded as the first channel routing algorithm
- Can be used in solving Channel Routing Problems
- Originally used in PCB design
- Can be applied on VLSI physical design
- Requires building the Vertical Constraint Graph (VCG) for a channel routing problem

Left-edge algorithm

Assumes one horizontal segment per net.

- Sweep pins from left to right:
  - assign horizontal segment to lowest available track.



Example