Moore’s Law

- Predicted that number of transistors per chip would grow exponentially (double every 18 months).
- Exponential improvement in technology is a natural trend: steam engines, dynamos, automobiles.

Moore’s Law plot

Choice of technology

- Two distinct types of technology are fabricated in silicon based upon
  - BJT (Bipolar Junction Transistor)
  - MOS (Metallic Oxide Semiconductor)
- Since processing of these technologies is very different, it is impractical to mix them up within a chip

Choice of MOS and BJT

- MOS logic occupies much smaller area of silicon than the equivalent BJT logic
- MOS technology has a much higher potential packing density
- A MOS logic circuit requires appreciably less current and hence less power than its bipolar counterpart
- However, bipolar circuits operate faster than MOS circuits
- Even so, the speed-power product for MOS logic compares favorably with that of BJT logic
**Terminology**

**Manufacturing node:** technology at a particular channel length. ---a new technology node every two years?

- **Micron**
- **Submicron**
- **Deep submicron technology:** 250-100 nm.
- **Nanometer technology:** 100 nm and below.

---

**Power Consumption Constraint**

The **large power consumption** of a CMOS logic circuit can limit the number of transistors on a single chip. This in turn changes system design in several ways.

- It increases the physical size of a system.
- Time required to transmit a signal between chips is much larger than the time required to send the same signal between two transistors on the same chip; lowers speed
- Electrical design of multi-chip systems becomes more complex:
  - Parasitics (resistance, **capacitance & inductance**) can cause a number of ringing effects that are much harder to analyze.

---

**Design and Testability**

...needed to check whether the designed chips have been manufactured correctly

- *verify or validate*
- manufacturing test

Unfortunately, not all chip designs are equally testable.

---

**Reliability**

*Reliability is a lifetime problem*

- Transient failures that cause occasional problems
- Permanent failures but only after the chip has operated for some time—*overheating*
- Other manufacturing problems cause problems that are harder to diagnose may affect performance rather than functionality.
The cost of fabrication

- Current cost: $4 billion.
- Typical fab line occupies about 1 city block, employs a few hundred people.
- Most profitable period is first 18 months-2 years.

Cost factors in ICs

- For large-volume ICs:
  - packaging is largest cost;
  - testing is second-largest cost.
- For low-volume ICs, design costs may swamp all manufacturing costs.

Cost of design

- Design cost can be significant: $20 million for a large ASIC, $500 million for a large CPU.
- Cost elements:
  - Architects, logic designers, etc.
  - CAD tools.
  - Computers the CAD tools run on.

The VLSI design process

- May be part of larger product design.
- Major levels of abstraction:
  - specification; what the chip does, inputs/outputs
  - architecture; major resources, connections
  - Register transfer; logic blocks, FSMs, connections
  - logic design; gates, flip-flops, latches,
  - circuit design; transistors, parasitics, connections
  - layout; mask layers, polygons
Challenges in VLSI design

- Multiple levels of abstraction: transistors to CPUs.
- Multiple and conflicting constraints: low cost and high performance are often at odds.
- Short design time: Late products are often irrelevant.

Dealing with design complexities

Designers have developed two techniques to eliminate unnecessary detail:

- Hierarchical design
- Design abstraction