Topics

- Basic fabrication steps.
- Transistor structures.
- Basic transistor behavior.
- Latch up.

Our technology

- Technology node: 500/180 nm
  - Assume 1.2V supply voltage.
- Parameters are typical values.

We need to study fabrication processes and the design rules that govern layout.

Fabrication services

- Educational services:
  - U.S.: MOSIS
  - EC: EuroPractice
  - Taiwan: CIC
  - Japan: VDEC
- Foundry = fabrication line for hire.
  - Foundries are major source of fab capacity today.

Fabrication processes

- IC is built on silicon substrate:
  - some structures diffused into substrate;
  - other structures built on top of substrate.
- Substrate regions are doped with n-type and p-type impurities. (n+ = heavily doped)
- Wires made of polycrystalline silicon (poly), multiple layers of aluminum (metal).
- Silicon dioxide (SiO₂) is insulator.
Forming components on Silicon

Components are formed by a combination of processes:

• doping the substrate with impurities to create areas such as the n⁺ and p⁺ regions;
• adding or cutting away insulating silicon dioxide, or SiO₂ on top of the substrate;
• adding wires made of polycrystalline silicon (*polysilicon, also known as poly*) or metal, insulated from the substrate by SiO₂.

Metal Oxide Semiconductor (MOS)

Simple cross section

Photolithography

Mask patterns are put on wafer using photosensitive material using light:
There are three ways to form tubs in a substrate:

- start with a p-doped wafer and add n-tubs;
- start with an n-doped wafer and add p-tubs;
- start with an undoped wafer and add both n- and p-tubs.

1. First place tubs to provide properly-doped substrate for n-type, p-type transistors:

   - p-tub
   - p-tub
   - substrate

2. Form an oxide covering of the wafer in two steps: Thick field oxide & Thin gate oxide

3. Pattern polysilicon before diffusion regions:

   - p-tub
   - gate oxide
   - poly

4. Add diffusions, performing self-masking and self-alignment:

   - poly
   - p-tub
   - n+ p-tub
   - p+ p-tub
5. Start adding metal layers:

- Metal 1
  - n+ p-tub n+ p-tub p+
  - Poly

0.25 micron transistor (Bell Labs)

- Gate oxide
- Source/drain
- Poly
- Silicide

Transistor layout

- n-type
  - n-type diffusion
  - Poly
  - Tub

This layout is of a minimum-size transistor