Topics

- Basic fabrication steps.
- Transistor structures.
- Basic transistor behavior.
- Latch up.

Our technology

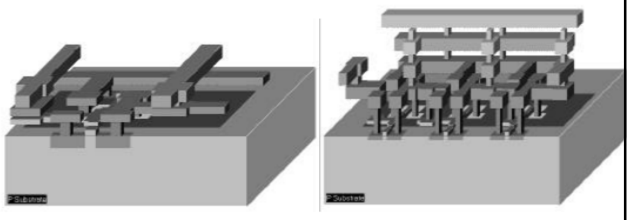
- Technology node: 500/180 nm
  - Assume 1.2V supply voltage.
- Parameters are typical values.

We need to study fabrication processes and the design rules that govern layout.

Fabrication services

- Educational services:
  - U.S.: MOSIS
  - EC: EuroPractice
  - Taiwan: CIC
  - Japan: VDEC
- Foundry = fabrication line for hire.
  - Foundries are major source of fab capacity today.

Evolution of the aspect of the integrated circuit



(a) 0.7µm *(b) 0.12µm technology*

Evolution of interconnect between 0.7µm technology and 0.12µm technology (Inv3.MSK)

Fabrication processes

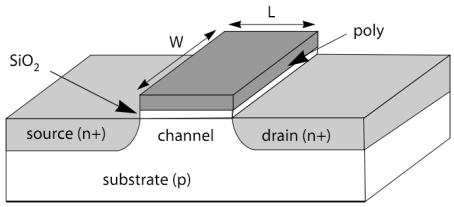
- IC is built on silicon substrate:
  - some structures diffused into substrate;
  - other structures built on top of substrate.
- Substrate regions are doped with n-type and p-type impurities. (n+ = heavily doped)
- Wires made of polycrystalline silicon (poly), multiple layers of aluminum (metal).
- Silicon dioxide (SiO_2) is insulator.

Forming components on Silicon

Components are formed by a combination of processes:

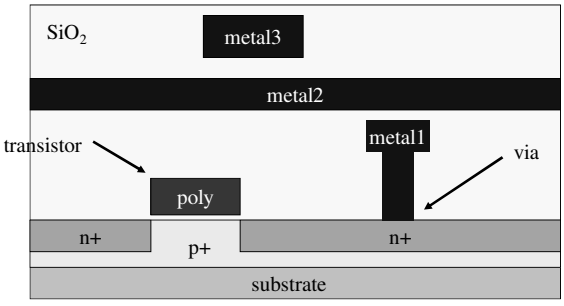
- doping the substrate with impurities to create areas such as the n^+ and p^+ regions;
- adding or cutting away insulating silicon dioxide, or SiO_2 on top of the substrate;
- adding wires made of polycrystalline silicon (***polysilicon, also known as poly***) or metal, insulated from the substrate by SiO_2

Metal Oxide Semiconductor (MOS)



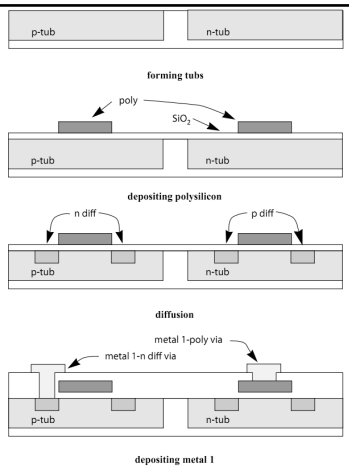
Cross-section of a MOS transistor

Simple cross section



Photolithography

Mask patterns are put on wafer using photo-sensitive material using light:

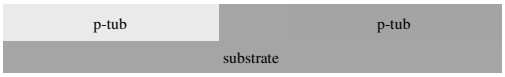


Twin-tub Fabrication Process

- There are three ways to form tubs in a substrate:
- start with a p-doped wafer and add n-tubs;
- start with an n-doped wafer and add p-tubs;
- start with an undoped wafer and add both n- and p-tubs.

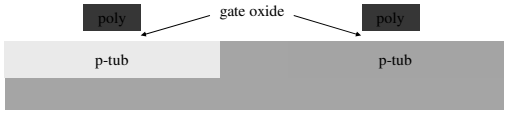
Process steps

1. First place tubs to provide properly-doped substrate for n-type, p-type transistors:



Process steps, cont'd.

2. Form an oxide covering of the wafer in two steps: Thick *field oxide* & Thin *gate oxide*
3. Pattern polysilicon before diffusion regions:

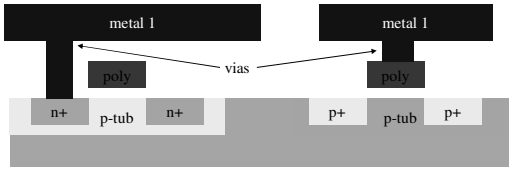


Process steps, cont'd

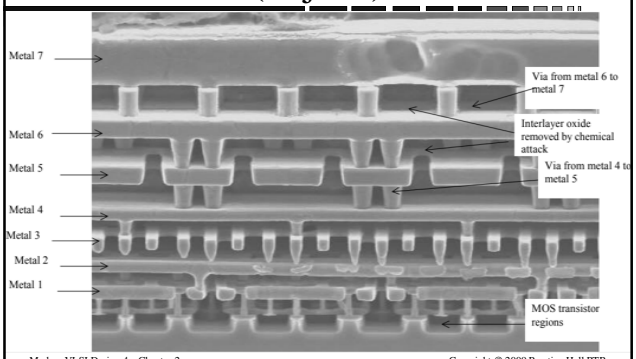
4. Add diffusions, performing self-masking and self-alignment:

Process steps, cont'd

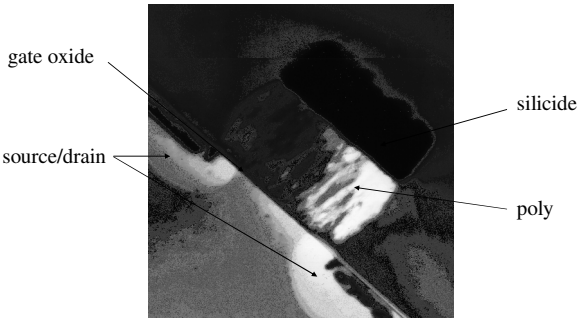
5. Start adding metal layers:



Cross-section of a 0.12µm technology (Fujitsu)

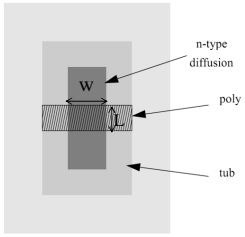


0.25 micron transistor (Bell Labs)



Transistor layout

n-type



This layout is of a minimum-size transistor.