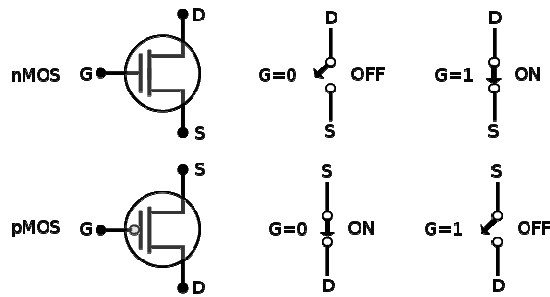


MOSFET



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A Simple Transistor Model

The variables that describe a transistor's behavior, are:

- V_{gs} —the gate-to-source voltage;
- V_{ds} —the drain-to-source voltage (remember that $V_{ds} = -V_{sd}$);
- I_d —the current flowing between the drain and source.

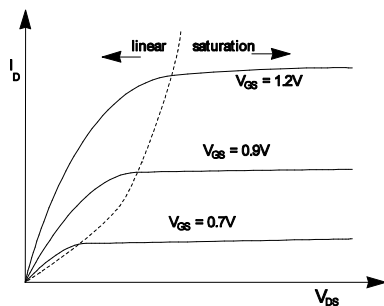
The constants that determine the magnitude of source-to-drain current in the transistor are:

- V_t —the transistor threshold voltage, which is positive for an n-type transistor and negative for a p-type transistor;
- k' —the transistor transconductance, which is positive for both types of transistors;
- W/L —the width-to-length ratio of the transistor.

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Drain current characteristics



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Drain current

- Linear region ($V_{ds} < V_{gs} - V_t$):
 $I_d = k' (W/L) [(V_{gs} - V_t)V_{ds} - 0.5 V_{ds}^2]$
- Saturation region ($V_{ds} \geq V_{gs} - V_t$):
 $I_d = 0.5k' (W/L)(V_{gs} - V_t)^2$

	k'	V_t
n-type	$k'_n = 170 \mu A/V^2$	$0.5V$
p-type	$k'_p = -30 \mu A/V^2$	$-0.5V$

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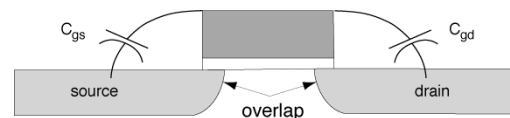
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A minimum-size transistor in the SCMOS rules is of size $L = 2\lambda$ and $W = 3\lambda$. Given this size of transistor and the 180 nm transistor characteristics, calculate the current through a minimum-sized n-type transistor at the boundary between the linear and saturation regions at $V_{gs} = 0.7V$

$$I_d = \frac{1}{2} \left(170 \frac{\mu A}{V^2} \right) \left(\frac{3\lambda}{2\lambda} \right) (0.7V - 0.5V)^2 = 5.1 \mu A$$

Basic transistor parasitics

1. Gate to substrate, also gate to source/drain.
2. Source/drain capacitance, resistance.



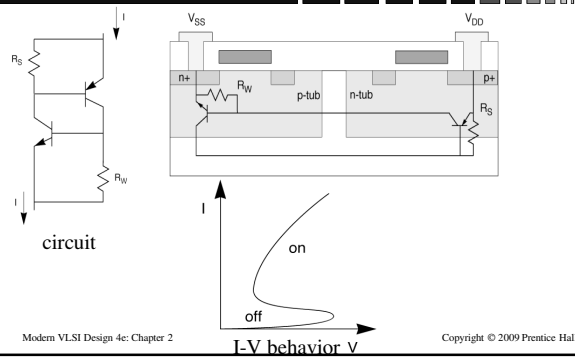
Basic transistor parasitics, cont'd

3. Gate capacitance C_g . Determined by active area.
4. Source/drain overlap capacitances C_{gs} , C_{gd} . Determined by source/gate and drain/gate overlaps. Independent of transistor L .
– $C_{gs} = C_{ol} W$
5. Gate/bulk overlap capacitance.

Latch-up

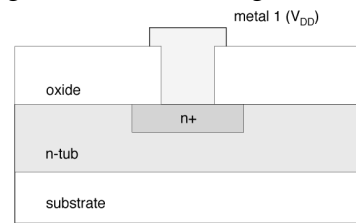
- CMOS ICs have parasitic silicon-controlled rectifiers (SCRs).
- When powered up, SCRs can turn on, creating low-resistance path from power to ground. Current can destroy chip.
- Early CMOS problem. Can be solved with proper circuit/layout structures.

6. Parasitic SCR



Solution to latch-up

Use tub ties to connect tub to power rail. Use enough to create low-voltage connection.



Tub tie layout

