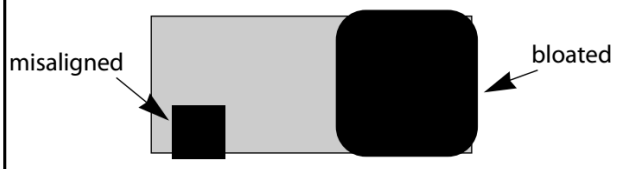
Design rules

What's happened?



Why we need design rules

Design rules for a process are formulated to minimize the occurrence of common fabrication problems and bring the yield of correct chips to an acceptable level

- Manufacturing processes have inherent limitations in accuracy.
- Design rules specify geometry of masks which will provide reasonable yields.
- Design rules are determined by experience.

Design rules and yield

- Design rules are determined by manufacturing process characteristics.
- Design rules should provide adequate yield if followed.
- Types of design rules:
  - ***Spacing***.
  - ***Separation***.
  - ***Composition***.

Manufacturing problems

- Photoresist shrinkage, tearing.
- Variations in material deposition.
- Variations in temperature.
- Variations in oxide thickness.
- Impurities.
- Variations between lots.
- Variations across a wafer.

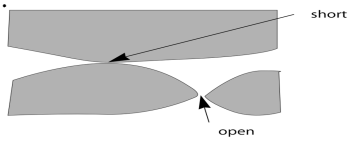
→
- Transistor problems
- Wiring problems
- Oxide problems
- Via problems

Transistor problems

- Varaiations in threshold voltage:
  - oxide thickness;
  - ion implanatation;
  - poly variations.
- Changes in source/drain diffusion overlap.
- Variations in substrate.

Wiring problems

- Diffusion: changes in doping -> variations in resistance, capacitance.
- Poly, metal: variations in height, width -> variations in resistance, capacitance.
- Shorts and opens:



Oxide problems

- Variations in height.
- Lack of planarity -> step coverage.

Via problems

- Via may not be cut all the way through.
- Undesize via has too much resistance.
- Via may be too large and create short.

Scaling theory

- In digital circuit design scaling is possible because the capacitive loads that must be driven by logic gates shrink faster than the currents supplied by the transistors.
- Classical scaling theory runs into complications at nanometer features.
  - Leakage.
  - Smaller supply voltage.

Scaling model

Assume that all the basic physical parameters of the chip are shrunk by a factor *1/x*:

- $\lambda \rightarrow \lambda /x$.
- $W \rightarrow W/x$, $L \rightarrow L/x$.
- $t_{ox} \rightarrow t_{ox} /x$.
- $N_d \rightarrow N_d/x$.
- $V_{DD} - V_{SS} \rightarrow (V_{DD} - V_{SS})/x$.

Current and capacitance scaling

$\hat{k}'/k' = x \quad \hat{V}_t = V_t/x$

$$\frac{\hat{I}_d}{I_d} = \left(\frac{\hat{k}'}{k'}\right)\left(\frac{\hat{W}/\hat{L}}{W/L}\right)\left[\frac{(\hat{V}_{gs}-\hat{V}_t)^2}{(V_{gs}-V_t)^2}\right]$$

$$= x\left(\frac{1/x}{1/x}\right)\left(\frac{1}{x}\right)^2 = \frac{1}{x}$$

- Saturation drain current scales as 1/x.
- Capacitance scales as 1/x.
- Total performance over scaling:
  - [C'V'/l']/[CV/l] = 1/x

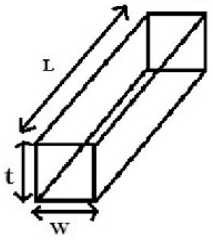
So, as the layout is scaled from λ to $\hat{\lambda} = \lambda/x$, ***the circuit is actually speeded up by a factor "x"***

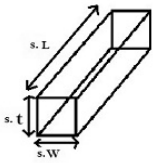
Interconnect scaling

- Two varieties of interconnect scaling:
  - **Ideal scaling** reduces vertical and horizontal dimensions equally: *the resistance increases with scaling*.
  - **Constant dimension** does not change wiring sizes: *resistance remains same*.
  - Higher levels of interconnect are constant dimension---same as older technologies.

https://www.vlsisystemdesign.com/kunal58625/php/scaling.php

Scaling of Resistance for Short Wires





Assume technology node as 180nm

R(180 nm) = constant (L / A)

R(180 nm) = constant (L / W.t)

Assume technology node as 130nm

R(130 nm) = constant (s.L / s.W.s.t)

R(130 nm) = constant (L / s.W.t)

R(130 nm) = (1/s) R(180 nm)

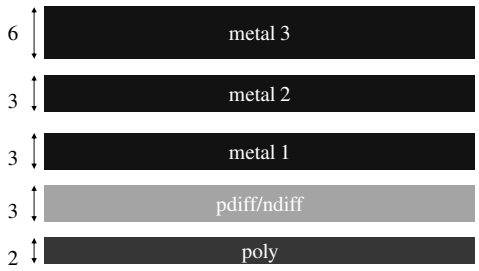
MOSIS SCMOS design rules

- Designed to scale across a wide range of technologies.
- Designed to support multiple vendors.
- Designed for educational use.
- Ergo, fairly conservative.

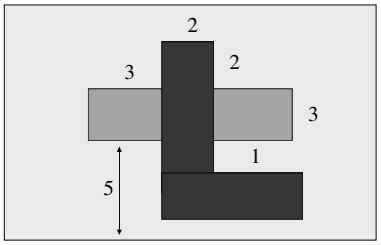
λ and design rules

- λ is the size of a minimum feature.
- Specifying λ particularizes the scalable rules.
- Parasitics are generally not specified in λ units.

Wires

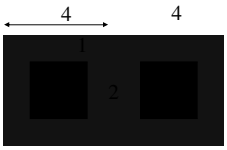


Transistors



Vias

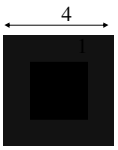
- Types of via: metal1/diff, metal1/poly, metal1/metal2.



Metal 3 via

- Type: metal3/metal2.
- Rules:
  - cut: 3 x 3
  - overlap by metal 2: 1
  - minimum spacing: 3
  - minimum spacing to via1: 2

Tub tie



Spacings

- Diffusion/diffusion: 3
- Poly/poly: 2
- Poly/diffusion: 1
- Via/via: 2
- Metal1/metal1: 3
- Metal2/metal2: 4
- Metal3/metal3: 4

Scmos VARIATIONS

	SCMOS	SCMOS submicron	SCMOS deep
Poly space	2	3	3
Active extension beyond poly	3	3	4
Contact space	2	3	4
Via width	2	2	3
Metal 1 space	2	3	3
Metal 2 space	3	3	4

Quize

Predict how metal 1 and metal 2 resistance would change for a 90 nm process using:

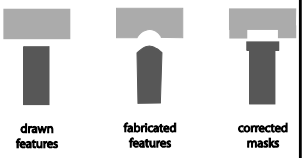
- a) Ideal scaling.
- b) Constant dimension scaling

Assignment

- What SIZE is required to make the saturation drain current of a p-type transistor approximately equal to the saturation drain current of a minimum-width n-type transistor?

Lithography for nanometer processes

- Optical proximity (Interference) causes drawn features to be distorted during lithography.
- Optical proximity correction pre-distorts masks so they create the proper features during lithography.

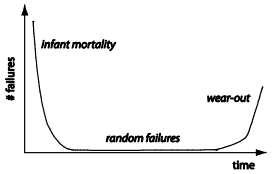


3-D integration

- 3-D technology stacks multiple levels of transistors and interconnect.
- Through-silicon-via (TSV) with die stacking uses special via to connect between separately fabricated chips.
- Multilayer buried structures build several layers of devices on a substrate.

Reliability

- Failures happen early, late in chip's life.
- Infant mortality is caused by marginal components.
- Late failures are caused by wear-out (metal migration, thermal, etc.).



Mean-time-to-failure

- MTF for metal wires = time required for 50% of wires to fail.
- Depends on current density:
  - proportional to $j^{-n}\ e^{\ Q/kT}$
  - j is current density
  - n is constant between 1 and 3
  - Q is diffusion activation energy
- Can determine lifetime from MTTF.

Traditional sources of unreliability

- Diffusions and junctions: crystal defects, impurity precipitation, mask misalignment, surface contamination.
- Oxides: Mobile ions, pinholes, interface states, hot carriers, time-dependent dielectric breakdown.
- Metalization: scratches/voids, mechanical damage, non-ohmic contacts, step coverage.

TDDB

- Time-dependent dielectric breakdown: gate voltages cause stress in gate oxides.
- More common as oxides become thinner.
- TDDB failure rate:
  - $MTTF = A\ 10^{\ \beta E}\ e^{Es/kt}$

Hot carriers

- Hot carrier has enough energy to jump from silicon to oxide.
- Accumulated hot carriers create a space charge that affects threshold voltage.

Electromigration and stress migration

- Degenerative failure for wires.
- Grains in metal have defects at grain surface that cause electromigration.
- Stress migration caused by mechanical stress.
  - Can occur even with zero current.

Soft errors

- Caused by alpha particles.
- Packages contain small amounts of uranium and thorium, which generate error-inducing radiation.