

**Lesson plan**  
for  
**CSE 1211: Introduction to Digital Electronics**  
**CSE 1212: Introduction to Digital Electronics LAB**  
1<sup>st</sup> year, Even Semester 2021

**Course Instructor:**

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**Office:** 4<sup>th</sup> Science building, Room No. 117

**Lectures:**

Sunday 9:20 am~ 10:20 am

Monday 9:20 am~ 10:20 am

Thursday 9:20 am~ 10:20 am

**Classroom:** 4<sup>th</sup> Science building, Room No. 313

**Laboratory Works:** Room No. 315

Thursday 10:25 am~ 12:30 pm

**Topics included:**

Logic Gates and Boolean Algebra, Number Systems, Switching Devices, Flip-Flops (FFs), 555 Time, and A/D And D/A Converters.

**Course materials:**

1. Text books:
  - i) Digital Systems: Principles and Applications, Ronald J. Tocci
2. Reference books:
  - i) An Introduction to Switching Theory and Digital Electronics, V. K. Jain

**Course outcome:** After completing the course the students

- will be able to understand both the fundamentals and also the design, implementation and application principles of digital electronics, devices and integrated circuits
- will also achieve a basic understanding of number systems and representations, different type of codes, logic gates and Boolean algebra, DTL, TTL and CMOS integrated circuits, basic combinational and sequential logic design, timer and A/D-D/A converters

**Prerequisite:** Fundamental knowledge of Basic Electronics and Introduction to Computer Systems

**Grading policy:**

Individual component of the class will be weighted as follows

Class attendance: 10%

Class test/ Assignment/ Continuous Assessment: 20%

Final Exam: 70%

Grading will be done on a straight mark basis.

**Exams:**

There will be three class test (CT) and a final exam in the course. No electronic device other than a calculator will be allowed during the exam (including phones, PDAs, MP3/CD players). The tentative dates of the exam are given below:

1<sup>st</sup> CT--- 02/09/2022

2<sup>nd</sup> CT---06/11/2022

3<sup>rd</sup>CT --- 01/12/202

Final Exam--- Date will be announced by the Faculty of Engineering

**Assignment:**

Assignments will be given periodically. The assignments are to be worked individually. Any work directly copied from the internet, other students, textbook etc. will result an automatic zero for the assignment. All late submission will have points deducted from them. Assignment must be returned as hand-written report. A week after the due date the assignments will no longer be accepted.

**Tentative class schedule:**

|                        |  |
|------------------------|--|
| 1 <sup>st</sup> week:  | Fundamentals of Digital Logic System and Number systems  |
| 2 <sup>nd</sup> week:  | Logic gates and Boolean algebra  |
| 3 <sup>rd</sup> week:  | Logic gates and Boolean algebra: Minimization Techniques   |
| 4 <sup>th</sup> week:  | Logic gates and Boolean algebra: Minimization Techniques   |
| 5 <sup>th</sup> week:  | Switching Devices  |
| 6 <sup>th</sup> week:  | Flip-Flops (FFs) and related devices   |
| 7 <sup>th</sup> week:  | Flip-Flops (FFs) and related devices   |
| 8 <sup>th</sup> week:  | 555 Timer  |
| 9 <sup>th</sup> week:  | A/D And D/A Converters   |
| 10 <sup>th</sup> week: | A/D And D/A Converters and Course reviews and discussion on question pattern for final examination |
| 11 <sup>th</sup> week: | Presentation on at least one assignment  |

## CSE 1212: Introduction to Digital Electronics LAB

| Tentative<br>LAB<br>schedule: | <b>LAB Programs</b>  |
|-------------------------------|--|
| 1 <sup>st</sup> week:         | To study and verify the truth table of logic gates   |
| 2 <sup>nd</sup> week:         | To Implementation of different logic function  |
| 3 <sup>rd</sup> week:         | To realize half/full adder and half/full subtractor.<br>i. Using X-OR and basic gates<br>ii. Using only NAND gates.                              |
| 4 <sup>th</sup> week:         | To verify BCD to excess –3 code conversion using NAND gates. To study and verify the truth table of excess-3 to BCD code converter. (Vice versa) |
| 5 <sup>th</sup> week:         | To convert given binary numbers to gray codes. (Vice versa)  |
| 6 <sup>th</sup> week:         | To implement Parity generator and checker<br>Truth table verification of Flip-Flops:<br>i. SR<br>ii. JK<br>iii. D- Type<br>iv. T- Type.          |
| 7 <sup>th</sup> week:         | Design and testing of Bistable, Monostable and Astable multivibrators using 555  |
| 8 <sup>th</sup> week:         | timer.   |
| 9 <sup>th</sup> week:         | Design and testing A/D and D/A converters  |
| 10 <sup>th</sup> week:        |  |
| 11 <sup>th</sup> week:        | Design and test DTL and TTL logic gates  |